APPENDIX A

Please amend claims 5, 41 - 62, 64 - 65, 67 - 69, 71, 73, 76 - 77, 79, 83 - 87, 89, 91, and 94, as follows:

--5. (Amended) A filter processor system comprising:

an analog input device generating [an] analog input [signal] information;

an analog to digital converter coupled to the analog input device and generating digital [signal samples] information in response to the analog input [signal] information; and

an integrated circuit stored program digital computer coupled to the analog to digital converter and generating an output [signal] information in response to the digital [signal samples] information, said integrated circuit stored program digital computer including

a) an integrated circuit read only memory storing a computer program,

b) an integrated circuit input circuit coupled to the integrated circuit read only memory and to the analog to digital converter and generating input [signal samples] information in response to the digital [signal samples] information and in response to the computer program,

b) an integrated circuit random access memory storing digital [signal samples] information,

c) an integrated circuit writing circuit coupled to the integrated circuit read only memory, the integrated circuit input circuit, and the integrated circuit random access memory and writing the input

[signal samples] information generated by the integrated circuit input logic to said integrated circuit random access memory in response to the computer program,

d) an integrated circuit accessing circuit coupled to the integrated circuit random access memory and to the integrated circuit read only memory and accessing digital [signal samples] information stored [by] in [said] the integrated circuit random access memory in response to the computer program,

e) an integrated circuit processing circuit coupled to the integrated circuit accessing circuit and to the integrated circuit read only memory and generating filter processed [signal samples] information by filter processing the digital [signal samples] information accessed by said accessing circuit in response to the computer program, and

c) an integrated circuit output circuit coupled to the integrated circuit processing circuit and to the integrated circuit read only memory and generating [an] output [signal] information in response to the filter processed [signal samples] information and in response to the computer program.

--41. (Amended) A filter processor system comprising:

an analog input device generating [an] analog input [signal] information;

an analog to digital converter coupled to the analog input device and generating digital [signal samples] information in response to the analog input [signal] information; and

a single integrated circuit chip stored program digital computer coupled to the analog to digital converter and generating digital output [signal samples] information in response to the digital [signal samples] information, wherein the single integrated circuit chip stored program digital computer is implemented on a single integrated circuit chip, and wherein the single integrated circuit chip stored program digital computer includes

a) an integrated circuit read only memory storing a computer program, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip,

b) an integrated circuit input circuit coupled to the integrated circuit read only memory and to the analog to digital converter and generating input [signal samples] information in response to the digital [signal samples] information and in response to the computer program, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip,

c) an integrated circuit random access memory storing computer [signal samples] information, wherein the integrated circuit random access memory is implemented on the single integrated circuit chip,

d) an integrated circuit writing circuit coupled to the integrated circuit read only memory, the integrated circuit input circuit, and the integrated circuit random access memory and writing the computer [signal samples] information to the integrated circuit random access memory in response to the input [signal samples] information and in response to the computer program, wherein the integrated circuit writing circuit is implemented on the single integrated circuit chip,

e) an integrated circuit accessing circuit coupled to the integrated circuit random access memory and to the integrated circuit read only memory and accessing computer [signal samples] information stored [by] in the integrated circuit random access memory in response to the computer program, wherein the integrated circuit accessing circuit is implemented on the single integrated circuit chip,

f) an integrated circuit processing circuit coupled to the integrated circuit accessing circuit and to the integrated circuit read only memory and generating filter processed [signal samples] information by filter processing the computer [signal samples] information accessed by the integrated circuit accessing circuit in response to the computer program, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and

g) an integrated circuit output circuit coupled to the integrated circuit processing circuit and to the integrated circuit read only memory and generating the digital output [signal samples] information in response to the filter processed [signal samples] information and in response to the computer program, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--42. (Amended) A filter processor system as set forth in claim 41, further comprising:

a sound circuit coupled to the integrated circuit output circuit and generating [an] electrical sound [signal] information in response to the digital output [signal samples] information; and

a sound transducer coupled to the sound circuit and generating an acoustic sound in response to the electrical sound [signal] information.

--43. (Amended) A filter processor system as set forth in claim 41, further comprising:

a display circuit coupled to the integrated circuit output circuit and generating a display [signal] information in response to the digital output [signal samples] information; and

a display monitor coupled to the display circuit and generating a display in response to the display [signal] information.

--44. (Amended) A filter processor system as set forth in claim 41, further comprising a digital to analog converter circuit coupled to the integrated circuit output circuit and generating [an] analog output [signal] information in response to the digital output [signal samples] information.

--45. (Amended) A filter processor system as set forth in claim 41, wherein the integrated circuit output circuit is an integrated circuit serial output circuit generating the digital output [signal samples] information as serial digital output [signal samples] information in response to the in response to the filter processed [signal samples] information and in response to the computer program.

--46. (Amended) A filter processor system as set forth in claim 41, wherein the analog to digital converter generates the digital [signal samples] information as serial digital [signal samples] information and wherein the integrated circuit input circuit is an integrated circuit serial input circuit coupled to the integrated circuit read only memory and to the analog to digital converter and generating the input [signal samples] information in response to the serial digital [signal samples] information and in response to the computer program.

--47. (Amended) A receiver system comprising:

an antenna generating [an] antenna [signal] information;

an amplifier coupled to the antenna and generating [an] amplified [signal] information in response to the antenna [signal] information;

a sampling circuit coupled to the amplifier and generating received [signal samples] information in response to the amplified [signal] information; and

a single integrated circuit chip signal processor coupled to the amplifier and generating output [signal samples] information in response to the received [signal samples] information, wherein the single integrated circuit chip signal processor is implemented on a single integrated circuit chip, and wherein the single integrated circuit chip signal processor includes

a) an integrated circuit read only memory storing a [signal] processing program, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip,

b) an integrated circuit input circuit coupled to the integrated circuit read only memory and to the sampling circuit and generating input [signal samples] information in response to the received [signal samples] information and in response to the [signal] processing program, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip,

c) an integrated circuit random access memory storing [signal] processor [signal samples] information, wherein the integrated circuit random access memory is implemented on the single integrated circuit chip,

d) an integrated circuit writing circuit coupled to the integrated circuit read only memory, the integrated circuit input circuit, and the integrated circuit random access memory and writing the [signal] processor [signal samples] information to the integrated circuit random access memory in response to the input [signal samples] information and in response to the [signal] processing program, wherein the integrated circuit writing circuit is implemented on the single integrated circuit chip,

e) an integrated circuit accessing circuit coupled to the integrated circuit random access memory and to the integrated circuit read only memory and generating accessed [signal samples] information by accessing the [signal] processor [signal samples] information from the integrated circuit random access memory in response to the [signal] processing program, wherein the integrated circuit accessing circuit is implemented on the single integrated circuit chip,

f) an integrated circuit processing circuit coupled to the integrated circuit accessing circuit and to the integrated circuit read only memory and generating filter processed [signal samples] information by filter processing the accessed [signal samples] information in response to the [signal] processing program, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and

g) an integrated circuit output circuit coupled to the integrated circuit processing circuit and to the integrated circuit read only memory and generating the output [signal samples] information in response to the filter processed [signal samples] information and in response to the [signal] processing program, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--48. (Amended) A receiver system as set forth in claim 47, further comprising:

a sound circuit coupled to the integrated circuit output circuit and generating [an] electrical sound [signal] information in response to the output [signal samples] information and

a sound transducer coupled to the sound circuit and generating an acoustic sound in response to the electrical sound [signal] information.

--49. (Amended) A receiver system as set forth in claim 47, further comprising:

a display circuit coupled to the integrated circuit output circuit and generating [a] display [signal] information in response to the output [signal samples] information and

a display monitor coupled to the display circuit and generating a display in response to the display [signal] information.

--50. (Amended) A receiver system comprising:

an antenna generating [an] antenna [signal] information;

an amplifier coupled to the antenna and generating [an] amplified [signal] information in response to the antenna [signal] information;

a sampling circuit coupled to the amplifier and generating received [signal samples] information in response to the amplified [signal] information;

a single integrated circuit chip signal processor coupled to the amplifier and generating output [signal samples] information in response to the received [signal samples] information, wherein the single integrated circuit chip signal processor is implemented on a single integrated circuit chip, and wherein the single integrated circuit chip signal processor includes

a) an integrated circuit read only memory storing a [signal] processing program, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip,

b) an integrated circuit input circuit coupled to the integrated circuit read only memory and to the sampling circuit and generating input [signal samples] information in response to the received [signal samples] information and in response to the [signal] processing program, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip,

c) an integrated circuit random access memory storing [signal] processor [signal samples] information, wherein the integrated circuit random access memory is implemented on the single integrated circuit chip,

d) an integrated circuit writing circuit coupled to the integrated circuit read only memory, the integrated circuit input circuit, and the integrated circuit random access memory and writing the [signal] processor [signal samples] information to the integrated circuit random access memory in response to the input [signal samples] information and in response to the [signal] processing program, wherein the integrated circuit writing circuit is implemented on the single integrated circuit chip,

e) an integrated circuit accessing circuit coupled to the integrated circuit random access memory and to the integrated circuit read only memory and generating accessed [signal samples] information by accessing the [signal] processor [signal samples] information from the integrated circuit random access memory in response to the [signal] processing program, wherein the integrated circuit accessing circuit is implemented on the single integrated circuit chip,

f) an integrated circuit processing circuit coupled to the integrated circuit accessing circuit and to the integrated circuit read only memory and generating filter processed [signal samples] information by filter processing the accessed [signal samples] information in response to the [signal] processing program, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and

g) an integrated circuit output circuit coupled to the integrated circuit processing circuit and to the integrated circuit read only memory and generating the output [signal samples] information in response to the filter processed [signal samples] information and in response to the [signal] processing program, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip; and

a digital to analog converter circuit coupled to the integrated circuit output circuit and generating [an] analog output [signal] information in response to the output [signal samples] information.

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--51. (Amended) A receiver system as set forth in claim 47, wherein the integrated circuit output circuit is an integrated circuit serial output circuit generating the output [signal samples] information as serial digital output [signal samples] information in response to the filter processed [signal samples] information and in response to the [signal] processing program.

--52. (Amended) A receiver system as set forth in claim 47, wherein the sampling circuit generates the received [signal samples] information as serial digital received [signal samples] information and wherein the integrated circuit input circuit is an integrated circuit serial input circuit coupled to the integrated circuit read only memory and to the sampling circuit and generating the input [signal samples] information in response to the serial digital received [signal samples] information and in response to the [signal] processing program.

--53. (Amended) A digital signal processor comprising:

a single integrated circuit chip having a digital signal processor implemented thereon;

an integrated circuit read only memory storing a [signal] processor program, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signal samples] information in response to the [signal] processor program, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit random access memory storing [signal] processor [signal samples] information, wherein the integrated circuit random access memory is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, the integrated circuit input circuit, and the integrated circuit random access memory and writing the [signal] processor [signal samples] information to the integrated circuit random access memory in response to the input [signal samples] information and in response to the [signal] processor program, wherein the integrated circuit writing circuit is implemented on the single integrated circuit chip;

an integrated circuit accessing circuit coupled to the integrated circuit random access memory and to the integrated circuit read only memory and accessing [signal] processor [signal samples] information stored [by] in the integrated circuit random access memory in response to the [signal] processor program, wherein the integrated circuit accessing circuit is implemented on the single integrated circuit chip;

an integrated circuit [signal] processing circuit coupled to the integrated circuit accessing circuit and to the integrated circuit read only memory and generating signal processed [signal samples] information by [signal] processing the [signal] processor [signal samples] information accessed by the integrated circuit accessing circuit in response to the [signal] processor program, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip; and

an integrated circuit output circuit coupled to the integrated circuit [signal] processing circuit and to the integrated circuit read only memory and generating the digital output [signal samples] information in response to the signal processed [signal samples] information and in response to the [signal] processor program, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--54. (Amended) A digital signal processor as set forth in claim 53, further comprising:

a sound circuit coupled to the integrated circuit output circuit and generating [an] electrical sound [signal] information in response to the output [signal samples] information and

a sound transducer coupled to the sound circuit and generating an acoustic sound in response to the electrical sound [signal] information.

--55. (Amended) A digital signal processor as set forth in claim 53, further comprising:

a display circuit coupled to the integrated circuit output circuit and generating [a] display [signal] information in response to the digital output [signal samples] information and

a display monitor coupled to the display circuit and generating a display in response to the display [signal] information.

--56. (Amended) A digital signal processor comprising:

a single integrated circuit chip having a digital signal processor implemented thereon;

an integrated circuit read only memory storing a [signal] processor program, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signal samples] information in response to the [signal] processor program, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit random access memory storing [signal] processor [signal samples] information, wherein the integrated circuit random access memory is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, the integrated circuit input circuit, and the integrated circuit random access memory and writing the [signal] processor [signal samples] information to the integrated circuit random access memory in response to the input [signal samples] information and in response to the [signal] processor program, wherein the integrated circuit writing circuit is implemented on the single integrated circuit chip;

an integrated circuit accessing circuit coupled to the integrated circuit random access memory and to the integrated circuit read only memory and accessing [signal] processor [signal samples] information stored [by] in the integrated circuit random access memory in response to the [signal] processor program, wherein the integrated circuit accessing circuit is implemented on the single integrated circuit chip;

an integrated circuit [signal] processing circuit coupled to the integrated circuit accessing circuit and to the integrated circuit read only memory and generating signal processed [signal samples] information by [signal] processing the [signal] processor [signal samples] information accessed by the integrated circuit accessing circuit in response to the [signal] processor program, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip;

an integrated circuit output circuit coupled to the integrated circuit [signal] processing circuit and to the integrated circuit read only memory and generating the digital output [signal samples] information in response to the signal processed [signal samples] information and in response to the [signal] processor program, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip; and

a digital to analog converter circuit coupled to the integrated circuit output circuit and generating [an] analog output [signal] information in response to the digital output [signal samples] information.

--57. (Amended) A digital signal processor as set forth in claim 53, wherein the integrated circuit output circuit is an integrated circuit serial output circuit generating the digital output [signal samples] information as serial digital output [signal samples] information in response to the filter processed [signal samples] information and in response to the [signal] processing program.

--58. (Amended) A digital signal processor as set forth in claim 53, wherein the integrated circuit input circuit is an integrated circuit serial input circuit coupled to the integrated circuit read only memory and generating the input [signal samples] information as serial input [signal samples] information and in response to the [signal] processing program.

--59. (Amended) A filter processor implemented on a single integrated circuit chip comprising:

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signals] information in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input [signals] information and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and to the integrated circuit multiplier circuit and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and to the integrated circuit adder circuit and generating output operands by outputting the filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--60. (Amended) A correlator filter processor implemented on a single integrated circuit chip comprising:

an integrated circuit read only memory storing correlator instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing correlator operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signals] information in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input [signals] information and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating correlation filtered operands in response to the correlator operands and in response to the correlator instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating correlation product operands by multiplying correlator operands in response to correlator instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and to the integrated circuit multiplier circuit and generating correlation filtered operands by adding the correlation product operands in response to the correlator instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and to the integrated circuit adder circuit and generating correlator output operands by outputting the correlator filtered operands in response to the correlator instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--61. (Amended) A filter processor implemented on a single integrated circuit chip as set forth in claim 59, further comprising:

an integrated circuit synchronization circuit generating synchronization [signals] information, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization [signal] information.

--62. (Amended) A filter processor implemented on a single integrated circuit chip comprising:

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signals] information in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and

writing operands into the integrated circuit alterable memory in response to the input [signals] information and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit iterative processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and iteratively generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit iterative processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit iterative processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and to the integrated circuit multiplier circuit and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and to the integrated circuit adder circuit and generating output operands by outputting the filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--63. A filter processor implemented on a single integrated circuit chip as set forth in claim 59, wherein the integrated circuit processing circuit is an integrated circuit multiple loop iterative processing circuit iteratively generating the filtered operands with multiple iterative loops.

--64. (Amended) A filter processor implemented on a single integrated circuit chip comprising:

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit dynamic random access alterable memory storing operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signals] information in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input [signals] information and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and to the integrated circuit multiplier circuit and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and to the integrated circuit adder circuit and generating output operands by outputting the filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--65. (Amended) A filter processor implemented on a single integrated circuit chip comprising:

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signal samples] information in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input [signal samples] information and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--66. A filter processor implemented on a single integrated circuit chip as set forth in claim 65:

wherein the filter processor is a correlator filter processor;

wherein the integrated circuit read only memory stores the instructions as correlator instructions;

wherein the integrated circuit alterable memory stores the operands as correlator operands;

wherein the integrated circuit processing circuit generates the filtered operands as correlation filtered operands in response to the correlator operands and in response to the correlator instructions, and

wherein the integrated circuit output circuit generates the output operands by outputting the correlation filtered operands in response to the instructions.

--67. (Amended) A filter processor implemented on a single integrated circuit chip as set forth in claim 65, further comprising:

an integrated circuit synchronization circuit generating a synchronization [signal] information, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization [signal] information.

--68. (Amended) A filter processor implemented on a single integrated circuit chip comprising:

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signal samples] information in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input [signal samples] information and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit iterative processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and iteratively generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--69. (Amended) A filter processor implemented on a single integrated circuit chip comprising:

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signal samples] <u>information</u> in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input [signal samples] information and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit multiple loop iterative processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and iteratively generating filtered operands with multiple iterative loops in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--70. A filter processor implemented on a single integrated circuit chip as set forth in claim 65, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further comprising a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory.

--71. (Amended) An integrated circuit filter processor comprising:

an integrated circuit read only memory storing instructions;

an integrated circuit alterable memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signals] information in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input [signals] information and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--72. An integrated circuit filter processor as set forth in claim 71:

wherein the filter processor is a correlator filter processor;

wherein the integrated circuit read only memory stores the instructions as correlator instructions;

wherein the integrated circuit alterable memory stores the operands as correlator operands;

wherein the integrated circuit processing circuit generates the filtered operands as correlation filtered operands in response to the correlator operands and in response to the correlator instructions, and

wherein the integrated circuit output circuit generates the output operands by outputting the correlation filtered operands in response to the instructions.

--73. (Amended) An integrated circuit filter processor as set forth in claim 71, further comprising:

an integrated circuit synchronization circuit generating synchronization [signals] information;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization [signal] information.

--74. An integrated circuit filter processor as set forth in claim 71, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands.

--75. An integrated circuit filter processor as set forth in claim 71, wherein the integrated circuit processing circuit is an integrated circuit multiple loop iterative processing circuit iteratively generating the filtered operands with multiple iterative loops.

--76. (Amended) An integrated circuit filter processor comprising:

an integrated circuit read only memory storing instructions;

an integrated circuit dynamic random access alterable memory dynamically storing operands;

a refresh circuit coupled to the integrated circuit dynamic random access alterable memory and refreshing the integrated circuit dynamic random access alterable memory;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signals] information in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input [signals] information and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--77. (Amended) An integrated circuit filter processor comprising:

an integrated circuit read only memory storing instructions;

an integrated circuit alterable memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signal samples] information in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input [signal samples] information and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the operands and in response to the instructions, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--78. An integrated circuit filter processor as set forth in claim 77:

wherein the filter processor is a correlator filter processor;

wherein the integrated circuit read only memory stores the instructions as correlator instructions;

wherein the integrated circuit alterable memory stores the operands as correlator operands;

wherein the integrated circuit processing circuit generates the filtered operands as correlation filtered operands in response to the correlator operands and in response to the correlator instructions, and

wherein the integrated circuit output circuit generates the output operands by outputting the correlation filtered operands in response to the instructions.

--79. (Amended) An integrated circuit filter processor as set forth in claim 77, further comprising:

an integrated circuit synchronization circuit generating a synchronization [signal] information;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization [signal] information.

--80. An integrated circuit filter processor as set forth in claim 77, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands.

--81. An integrated circuit filter processor as set forth in claim 77, wherein the integrated circuit processing circuit is an integrated circuit multiple loop iterative processing circuit iteratively generating the filtered operands with multiple iterative loops.

--82. An integrated circuit filter processor as set forth in claim 77, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further comprising a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory.

--83. (Amended) An integrated circuit filter processor comprising:

an integrated circuit read only memory storing instructions;

an integrated circuit dynamic random access memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signals] information in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit dynamic random access memory and writing operands into the integrated circuit dynamic random access memory in response to the input [signals] information and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions;

an integrated circuit refresh circuit coupled to the integrated circuit dynamic random access memory and refreshing the integrated circuit dynamic random access memory; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--84. (Amended) An integrated circuit filter processor comprising:

an analog to digital converter generating digital converter [signals] information in response to analog input [signals] information;

an integrated circuit read only memory storing instructions;

an integrated circuit dynamic random access memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and to the analog to digital converter and generating input [signals] information in response to the instructions and in response to the digital converter [signals] information;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit dynamic random access memory and writing operands into the integrated circuit dynamic random access memory in response to the input [signals] information and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions;

an integrated circuit refresh circuit coupled to the integrated circuit dynamic random access memory and refreshing the integrated circuit dynamic random access memory; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--85. (Amended) An integrated circuit filter processor comprising:

an integrated circuit read only memory storing instructions;

an integrated circuit dynamic random access memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signals] information in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit dynamic random access memory and writing operands into the integrated circuit dynamic random access memory in response to the input [signals] information and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions;

an integrated circuit refresh circuit coupled to the integrated circuit dynamic random access memory and refreshing the integrated circuit dynamic random access memory;

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions; and

a digital to analog converter coupled to the integrated circuit output circuit and generating [an] analog output [signal] information in response to the output operands.

--86. (Amended) An integrated circuit filter processor comprising:

an integrated circuit read only memory storing instructions;

an integrated circuit dynamic random access memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input [signals] information in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit dynamic random access memory and writing operands into the integrated circuit dynamic random access memory in response to the input [signals] information and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit dynamic random access memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions;

an integrated circuit refresh circuit coupled to the integrated circuit dynamic random access memory and refreshing the integrated circuit dynamic random access memory;

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions;

a digital to analog converter coupled to the integrated circuit output circuit and generating [an] analog output [signal] information in response to the output operands; and

a display coupled to the digital to analog converter and displaying information in response to the analog output [signal] information.

--87. (Amended) An integrated circuit filter processor system comprising:

an analog to digital converter generating digital communication [signals] information in response to analog communications input [signals] information;

an integrated circuit read only memory storing instructions;

an integrated circuit alterable memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input communications [signals] information in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input communications [signals] information and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the communications operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying communications operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--88. An integrated circuit filter processor system as set forth in claim 87:

wherein the filter processor is a correlator filter processor;

wherein the integrated circuit read only memory stores the instructions as correlator instructions;

wherein the integrated circuit alterable memory stores the operands as correlator operands;

wherein the integrated circuit processing circuit generates the filtered operands as correlation filtered operands in response to the correlator operands and in response to the correlator instructions, and

wherein the integrated circuit output circuit generates the output operands by outputting the correlation filtered operands in response to the instructions.

--89. (Amended) An integrated circuit filter processor system as set forth in claim 87, further comprising:

an integrated circuit synchronization circuit generating synchronization [signals] information;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization [signal] information.

--90. An integrated circuit filter processor system as set forth in claim 87, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands.

--91. (Amended) An integrated circuit filter processor system comprising:

an analog to digital converter generating digital communication [signals] information in response to analog communications input [signals] information;

an integrated circuit read only memory storing instructions;

an integrated circuit alterable memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input communications [signals] information in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input communications [signals] information and in response to the instructions;

an integrated circuit multiple loop iterative processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and iteratively generating filtered operands with multiple iterative loops in response to the communications operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying communications operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--92. An integrated circuit filter processor system as set forth in claim 87, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further comprising a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory.

--93. An integrated circuit filter processor as set forth in claim 86,

wherein the filter processor is a correlator filter processor;

wherein the integrated circuit read only memory stores the instructions as correlator instructions;

wherein the integrated circuit alterable memory stores the operands as correlator operands;

wherein the integrated circuit processing circuit generates the filtered operands as correlation filtered operands in response to the correlator operands and in response to the correlator instructions, and

wherein the integrated circuit output circuit generates the output operands by outputting the correlation filtered operands in response to the instructions.

--94. (Amended) An integrated circuit filter processor as set forth in claim 86, further comprising:

an integrated circuit synchronization circuit generating synchronization [signals] information;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization [signal] information.

--95. An integrated circuit filter processor as set forth in claim 86, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands.

--96. An integrated circuit filter processor as set forth in claim 86, wherein the integrated circuit processing circuit is an integrated circuit multiple loop iterative processing circuit iteratively generating the filtered operands with multiple iterative loops.

--97. An integrated circuit filter processor as set forth in claim 86, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further comprising a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory.

Please add new claim 98 - 351, as follows:

--98. A digital signal processor comprising:

an integrated circuit operand memory storing computer operands;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

an integrated circuit read only memory storing a computer program comprising computer instructions;

an integrated circuit read only memory address circuit generating instruction addresses;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit; and

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit.

--99. A digital signal processor as set forth in claim 98, the integrated circuit instruction execution circuit comprising:

an input circuit generating input information;

a synchronization circuit generating synchronization information;

a loop heading circuit generating loop heading information;

a loop initializing circuit initializing loop information in response to the loop heading information and in response to the synchronization information;

a loop looping circuit looping through a loop in response to the loop information;

a skipping circuit skipping at least one loop through the loop in response to the loop information;

a loop update circuit generating updated loop information in response to the looping through the loop;

a first output circuit generating product information in response to the input information and in response to the updated loop information;

a second output circuit generating output rounded off product information in response to the product information; and

a loop exiting circuit exiting the loop in response to the updated loop information.

--100. A system comprising the digital signal processor as set forth in claim 98, the system further comprising;

a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the processed information generated by the integrated circuit instruction execution circuit; and

a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller.

--101. A system comprising the digital signal processor as set forth in claim 98, the system further comprising;

a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the processed information generated by the integrated circuit instruction execution circuit.

--102. A system comprising the digital signal processor as set forth in claim 98, the system further comprising;

a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit.

--103. A system comprising the digital signal processor as set forth in claim 98, the system further comprising;

a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the processed information generated by the integrated circuit instruction execution circuit; and

a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit.

--104. A digital signal processor comprising:

an integrated circuit operand memory storing computer operands;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

an integrated circuit read only memory storing a computer program comprising computer instructions;

an integrated circuit read only memory address circuit generating instruction addresses;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit; and

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit instruction execution circuit comprising:

an integrated circuit input circuit generating input information,

an outer loop header circuit generating outer loop header information,

an outer loop initializing circuit initializing outer loop information in response to the outer loop header information,

an outer loop looping circuit looping through an outer loop in response to the outer loop information,

an outer loop update circuit generating updated outer loop information in response to the looping through the outer loop,

a middle loop header circuit generating middle loop header information,

a middle loop initializing circuit initializing middle loop information in response to the middle loop header information and in response to the updated outer loop information,

a middle loop looping circuit looping through a middle loop in response to the middle loop information,

a middle loop update circuit generating updated middle loop information in response to the looping through the middle loop,

an inner loop header circuit generating inner loop header information,

an inner loop initializing circuit initializing inner loop information in response to the inner loop header information and in response to the updated middle loop information,

an inner loop looping circuit looping through an inner loop in response to the inner loop information,

a skipping circuit skipping at least one loop through the inner loop in response to the inner loop information,

an inner loop update circuit generating updated inner loop information in response to the looping through the inner loop,

a first output circuit generating change information in response to the input information and in response to the updated inner loop information, and

a second output circuit generating output rounded off change information in response to the change information.

105. A system comprising the digital signal processor as set forth in claim 104, the system further comprising;

a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller.

--106. A system comprising the digital signal processor as set forth in claim 104, the system further comprising;

a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the first processed information generated by the integrated circuit instruction execution circuit.

--107. A system comprising the digital signal processor as set forth in claim 104, the system further comprising;

a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit.

--108. A system comprising the digital signal processor as set forth in claim 104, the system further comprising;

a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit.

--109. A digital signal processor comprising:

an integrated circuit operand memory storing computer operands;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

an integrated circuit read only memory storing a computer program comprising computer instructions and storing an interrupt program comprising interrupt instructions;

an integrated circuit read only memory address circuit generating instruction addresses;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit interrupt input circuit generating input interrupt information;

an integrated circuit interrupt execution circuit coupled to the integrated circuit instruction execution circuit and coupled to the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit interrupting the generating of the first processed information by the integrated circuit instruction execution circuit in response to the input interrupt information generated by the integrated circuit interrupt input circuit;

an integrated circuit operand memory writing circuit coupled to the integrated circuit operand memory and coupled to the integrated circuit interrupt input circuit, the integrated circuit operand memory writing circuit writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit operand memory storing the interrupt return instruction address written by the integrated circuit operand memory writing circuit;

an integrated circuit interrupt address circuit generating an input interrupt address;

the integrated circuit read only memory address circuit further coupled to the integrated circuit interrupt address circuit and generating interrupt instruction addresses in response to the input interrupt address generated by the integrated circuit interrupt address circuit;

the integrated circuit read only memory accessing circuit generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit instruction execution circuit generating interrupt information in response to the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit and generating interrupt return information in response to at least one of the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit operand memory accessing circuit further coupled to the integrated circuit instruction execution circuit and generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information generated by the integrated circuit instruction execution circuit; and

the integrated circuit instruction execution circuit further generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit.

--110. A system comprising the digital signal processor as set forth in claim 109, the system further comprising;

a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the first processed information generated by the integrated circuit instruction execution circuit.

--111. A digital signal processor comprising:

an integrated circuit operand memory storing computer operands;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

an integrated circuit read only memory storing a computer program comprising computer instructions;

an integrated circuit read only memory address circuit generating instruction addresses;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit direct transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating direct transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit read only memory accessing circuit generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information generated by the integrated circuit direct transfer circuit; and

the integrated circuit instruction execution circuit generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed directly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

--112. A system comprising the digital signal processor as set forth in claim 111, the system further comprising;

a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit.

--113. A digital signal processor comprising:

an integrated circuit operand memory storing computer operands;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

an integrated circuit read only memory storing a computer program comprising computer instructions and storing an interrupt program comprising interrupt instructions;

an integrated circuit read only memory address circuit generating instruction addresses;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first

processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit interrupt input circuit generating input interrupt information;

an integrated circuit interrupt execution circuit coupled to the integrated circuit instruction execution circuit and coupled to the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit interrupting the generating of the first processed information by the integrated circuit instruction execution circuit in response to the input interrupt information generated by the integrated circuit interrupt input circuit;

an integrated circuit operand memory writing circuit coupled to the integrated circuit operand memory and coupled to the integrated circuit interrupt input circuit, the integrated circuit operand memory writing circuit writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit operand memory storing the interrupt return instruction address written by the integrated circuit operand memory writing circuit;

an integrated circuit interrupt address circuit generating an input interrupt address;

the integrated circuit read only memory address circuit further coupled to the integrated circuit interrupt address circuit and generating interrupt instruction addresses in response to the input interrupt address generated by the integrated circuit interrupt address circuit;

the integrated circuit read only memory accessing circuit generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit instruction execution circuit generating interrupt information in response to the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit and generating interrupt return information in response to at least one of the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit operand memory accessing circuit further coupled to the integrated circuit instruction execution circuit and generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information generated by the integrated circuit instruction execution circuit;

the integrated circuit instruction execution circuit further generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit index memory storing an index operand;

an integrated circuit indexing circuit coupled to the integrated circuit read only memory address circuit and coupled to the integrated circuit index memory, the integrated circuit indexing circuit generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indexing circuit and generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address generated by the integrated circuit indexing circuit; and

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indexed computer instructions generated by the integrated circuit read only memory accessing circuit.

--114. A system comprising the digital signal processor as set forth in claim 113, the system further comprising;

a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit.

--115. A digital signal processor comprising:

an integrated circuit operand memory storing computer operands;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

an integrated circuit read only memory storing a computer program comprising computer instructions;

an integrated circuit read only memory address circuit generating instruction addresses;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit index memory storing an index operand;

an integrated circuit indexing circuit coupled to the integrated circuit read only memory address circuit and coupled to the integrated circuit index memory, the integrated circuit indexing circuit generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indexing circuit and generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address generated by the integrated circuit indexing circuit;

the integrated circuit instruction execution circuit generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indexed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit direct transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating direct transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit read only memory accessing circuit generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information generated by the integrated circuit direct transfer circuit;

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed directly transferred computer instruction generated by the integrated circuit read only memory accessing circuit;

an integrated circuit indirect transfer memory storing an indirect transfer address;

an integrated circuit indirect transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating indirect transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indirect transfer memory and generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the

integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information generated by the integrated circuit indirect transfer circuit; and

the integrated circuit instruction execution circuit generating fourth processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indirectly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

--116. A system comprising the digital signal processor as set forth in claim 115, the system further comprising;

a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller.

--117. A digital signal processor comprising:

an integrated circuit operand memory storing computer operands;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

an integrated circuit read only memory storing a computer program comprising computer instructions;

an integrated circuit read only memory address circuit generating instruction addresses;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit index memory storing an index operand;

an integrated circuit indexing circuit coupled to the integrated circuit read only memory address circuit and coupled to the integrated circuit index memory, the integrated circuit indexing circuit generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indexing circuit and generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address generated by the integrated circuit indexing circuit;

the integrated circuit instruction execution circuit generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indexed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit indirect transfer memory storing an indirect transfer address;

an integrated circuit indirect transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating indirect transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indirect transfer memory and generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information generated by the integrated circuit indirect transfer circuit; and

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indirectly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

118. A system comprising the digital signal processor as set forth in claim 117, the system further comprising;

a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the first processed information generated by the integrated circuit instruction execution circuit.

--119. A digital signal processor comprising:

an integrated circuit operand memory storing computer operands;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

an integrated circuit read only memory storing a computer program comprising computer instructions;

an integrated circuit read only memory address circuit generating instruction addresses;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit index memory storing an index operand;

an integrated circuit indexing circuit coupled to the integrated circuit read only memory address circuit and coupled to the integrated circuit index memory, the integrated circuit indexing circuit generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indexing circuit and generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address generated by the integrated circuit indexing circuit;

the integrated circuit instruction execution circuit generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indexed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit direct transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating direct transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit read only memory accessing circuit generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information generated by the integrated circuit direct transfer circuit; and

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed directly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

--120. A system comprising the digital signal processor as set forth in claim 119, the system further comprising;

a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit.

--121. A digital signal processor comprising:

an integrated circuit operand memory storing computer operands;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

an integrated circuit read only memory storing a computer program comprising computer instructions and storing an interrupt program comprising interrupt instructions;

an integrated circuit read only memory address circuit generating instruction addresses;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit interrupt input circuit generating input interrupt information;

an integrated circuit interrupt execution circuit coupled to the integrated circuit instruction execution circuit and coupled to the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit interrupting the generating of the first processed information by the integrated circuit instruction execution circuit in response to the input interrupt information generated by the integrated circuit interrupt input circuit;

an integrated circuit operand memory writing circuit coupled to the integrated circuit operand memory and coupled to the integrated circuit interrupt input circuit, the integrated circuit operand memory writing circuit writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit operand memory storing the interrupt return instruction address written by the integrated circuit operand memory writing circuit;

an integrated circuit interrupt address circuit generating an input interrupt address;

the integrated circuit read only memory address circuit further coupled to the integrated circuit interrupt address circuit and generating interrupt instruction addresses in response to the input interrupt address generated by the integrated circuit interrupt address circuit;

the integrated circuit read only memory accessing circuit generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit instruction execution circuit generating interrupt information in response to the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit and generating interrupt return information in response to at least one of the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit operand memory accessing circuit further coupled to the integrated circuit instruction execution circuit and generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information generated by the integrated circuit instruction execution circuit;

the integrated circuit instruction execution circuit further generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit index memory storing an index operand;

an integrated circuit indexing circuit coupled to the integrated circuit read only memory address circuit and coupled to the integrated circuit index memory, the integrated circuit indexing circuit generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indexing circuit and generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address generated by the integrated circuit indexing circuit;

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indexed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit direct transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating direct transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit read only memory accessing circuit generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information generated by the integrated circuit direct transfer circuit; and

the integrated circuit instruction execution circuit generating fourth processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed directly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

122. A system comprising the digital signal processor as set forth in claim 121, the system further comprising;

a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit.

--123. A digital signal processor comprising:

an integrated circuit operand memory storing computer operands;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

an integrated circuit read only memory storing a computer program comprising computer instructions and storing an interrupt program comprising interrupt instructions;

an integrated circuit read only memory address circuit generating instruction addresses;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit interrupt input circuit generating input interrupt information;

an integrated circuit interrupt execution circuit coupled to the integrated circuit instruction execution circuit and coupled to the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit interrupting the generating of the first processed information by the integrated circuit instruction execution circuit in response to the input interrupt information generated by the integrated circuit interrupt input circuit;

an integrated circuit operand memory writing circuit coupled to the integrated circuit operand memory and coupled to the integrated circuit interrupt input circuit, the integrated circuit operand memory writing circuit writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit operand memory storing the interrupt return instruction address written by the integrated circuit operand memory writing circuit;

an integrated circuit interrupt address circuit generating an input interrupt address;

the integrated circuit read only memory address circuit further coupled to the integrated circuit interrupt address circuit and generating interrupt instruction addresses in response to the input interrupt address generated by the integrated circuit interrupt address circuit;

the integrated circuit read only memory accessing circuit generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit instruction execution circuit generating interrupt information in response to the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit and generating interrupt return information in response to at least one of the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit operand memory accessing circuit further coupled to the integrated circuit instruction execution circuit and generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information generated by the integrated circuit instruction execution circuit;

the integrated circuit instruction execution circuit further generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit index memory storing an index operand;

an integrated circuit indexing circuit coupled to the integrated circuit read only memory address circuit and coupled to the integrated circuit index memory, the integrated circuit indexing circuit generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indexing circuit and generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address generated by the integrated circuit indexing circuit;

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indexed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit indirect transfer memory storing an indirect transfer address;

an integrated circuit indirect transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating indirect transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indirect transfer memory and generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information generated by the integrated circuit indirect transfer circuit; and

the integrated circuit instruction execution circuit generating fourth processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indirectly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

124. A system comprising the digital signal processor as set forth in claim 123, the system further comprising;

a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit.

--125. A digital signal processor comprising:

an integrated circuit operand memory storing computer operands;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

an integrated circuit read only memory storing a computer program comprising computer instructions and storing an interrupt program comprising interrupt instructions;

an integrated circuit read only memory address circuit generating instruction addresses;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit interrupt input circuit generating input interrupt information;

an integrated circuit interrupt execution circuit coupled to the integrated circuit instruction execution circuit and coupled to the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit interrupting the generating of the first processed information by the integrated circuit instruction execution circuit in response to the input interrupt information generated by the integrated circuit interrupt input circuit;

an integrated circuit operand memory writing circuit coupled to the integrated circuit operand memory and coupled to the integrated circuit interrupt input circuit, the integrated circuit operand memory writing circuit writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit operand memory storing the interrupt return instruction address written by the integrated circuit operand memory writing circuit;

an integrated circuit interrupt address circuit generating an input interrupt address;

the integrated circuit read only memory address circuit further coupled to the integrated circuit interrupt address circuit and generating interrupt instruction addresses in response to the input interrupt address generated by the integrated circuit interrupt address circuit;

the integrated circuit read only memory accessing circuit generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit instruction execution circuit generating interrupt information in response to the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit and generating interrupt return information in response to at least one of the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit operand memory accessing circuit further coupled to the integrated circuit instruction execution circuit and generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information generated by the integrated circuit instruction execution circuit;

the integrated circuit instruction execution circuit further generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit index memory storing an index operand;

an integrated circuit indexing circuit coupled to the integrated circuit read only memory address circuit and coupled to the integrated circuit index memory, the integrated circuit indexing circuit generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indexing circuit and generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address generated by the integrated circuit indexing circuit;

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indexed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit direct transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating direct transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit read only memory accessing circuit generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information generated by the integrated circuit direct transfer circuit;

the integrated circuit instruction execution circuit generating fourth processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed directly transferred computer instruction generated by the integrated circuit read only memory accessing circuit;

an integrated circuit indirect transfer memory storing an indirect transfer address;

an integrated circuit indirect transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating indirect transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indirect transfer memory and generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the

integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information generated by the integrated circuit indirect transfer circuit; and

the integrated circuit instruction execution circuit generating fifth processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indirectly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

--126. A digital signal processor as set forth in claim 125, the integrated circuit instruction execution circuit comprising:

an input circuit generating input information;

a synchronization circuit generating synchronization information;

a loop header circuit generating loop header information;

a loop initializing circuit initializing loop information in response to the loop header information and in response to the synchronization information;

a loop looping circuit looping through a loop in response to the loop information;

a skipping circuit skipping at least one loop through the loop in response to the loop information;

a loop update circuit updating the loop information in response to the looping through the loop;

a first output circuit generating change information in response to the input information and in response to the looping through the loop; and

a second output circuit generating output rounded off change information in response to the change information.

--127. A system comprising the digital signal processor as set forth in claim 125, the system further comprising;

a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller.

--128. A system comprising the digital signal processor as set forth in claim 125, the system further comprising;

a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the first processed information generated by the integrated circuit instruction execution circuit.

--129. A system comprising the digital signal processor as set forth in claim 125, the system further comprising;

a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit.

--130. A system comprising the digital signal processor as set forth in claim 125, the system further comprising;

a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit.

--131. An integrated circuit digital signal processor implemented on a single integrated circuit chip, the integrated circuit digital signal processor comprising:

an integrated circuit operand memory storing computer operands, the integrated circuit operand memory implemented on the single integrated circuit chip;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory, the integrated circuit operand memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory storing a computer program comprising computer instructions, the integrated circuit read only memory implemented on the single integrated circuit chip;

an integrated circuit read only memory address circuit generating instruction addresses, the integrated circuit read only memory address circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit implemented on the single integrated circuit chip;

an integrated circuit index memory storing an index operand, the integrated circuit index memory implemented on the single integrated circuit chip;

an integrated circuit indexing circuit coupled to the integrated circuit read only memory address circuit and coupled to the integrated circuit index memory, the integrated circuit indexing circuit generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses generated by the integrated circuit read only memory address circuit, the integrated circuit indexing circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indexing circuit and generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address generated by the integrated circuit indexing circuit; and

the integrated circuit instruction execution circuit generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indexed computer instructions generated by the integrated circuit read only memory accessing circuit.

--132. A system comprising the integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 131, the system further comprising:

a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller.

--133. An integrated circuit digital signal processor implemented on a single integrated circuit chip, the integrated circuit digital signal processor comprising:

an integrated circuit operand memory storing computer operands, the integrated circuit operand memory implemented on the single integrated circuit chip;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory, the integrated circuit operand memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory storing a computer program comprising computer instructions, the integrated circuit read only memory implemented on the single integrated circuit chip;

an integrated circuit read only memory address circuit generating instruction addresses, the integrated circuit read only memory address circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the

integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit implemented on the single integrated circuit chip; and

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit implemented on the single integrated circuit chip.

#1
F24

--134. An integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 133, the integrated circuit instruction execution circuit comprising:

an input circuit generating input information;

a synchronization circuit generating synchronization information;

a frame loop header circuit generating frame loop header information;

a frame loop initializing circuit initializing frame loop information in response to the frame loop header information and in response to the synchronization information;

a frame loop looping circuit looping through a frame loop in response to the frame loop information;

a frame loop update circuit generating updated frame loop information in response to the looping through the frame loop;

a block loop header circuit generating block loop header information;

a block loop initializing circuit initializing block loop information in response to the block loop header information and in response to the updated frame loop information;

a block loop looping circuit looping through a block loop in response to the block loop information;

a block loop update circuit generating updated block loop information in response to the looping through the block loop;

a sample loop header circuit generating sample loop header information;

a sample loop initializing circuit initializing sample loop information in response to the sample loop header information and in response to the updated block loop information;

a sample loop looping circuit looping through a sample loop in response to the sample loop information;

a skipping circuit skipping at least one loop through the sample loop in response to the sample loop information;

a sample loop update circuit generating updated sample loop information in response to the looping through the sample loop;

a first output circuit generating product information in response to the input information and in response to the updated sample loop information; and

a second output circuit generating output rounded off product information in response to the product information.

--135. A system comprising the integrated circuit digital signal processor as set forth in claim 133, the system further comprising:

a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the processed information generated by the integrated circuit instruction execution circuit; and

a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller.

--136. A system comprising the integrated circuit digital signal processor as set forth in claim 133, the system further comprising:

a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the processed information generated by the integrated circuit instruction execution circuit.

--137. A system comprising the integrated circuit digital signal processor as set forth in claim 133, the system further comprising:

a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit.

--138. A system comprising the integrated circuit digital signal processor as set forth in claim 133, the system further comprising:

a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the processed information generated by the integrated circuit instruction execution circuit; and

a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit.

--139. An integrated circuit digital signal processor implemented on a single integrated circuit chip, the integrated circuit digital signal processor comprising:

an integrated circuit operand memory storing computer operands, the integrated circuit operand memory implemented on the single integrated circuit chip;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory, the integrated circuit operand memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory storing a computer program comprising computer instructions, the integrated circuit read only memory implemented on the single integrated circuit chip;

an integrated circuit read only memory address circuit generating instruction addresses, the integrated circuit read only memory address circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit implemented on the single integrated circuit chip;

an integrated circuit indirect transfer memory storing an indirect transfer address, the integrated circuit indirect transfer memory implemented on the single integrated circuit chip;

an integrated circuit indirect transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating indirect transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit indirect transfer circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indirect transfer memory and generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information generated by the integrated circuit indirect transfer circuit; and

the integrated circuit instruction execution circuit generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indirectly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

140. A system comprising the integrated circuit digital signal processor as set forth in claim 139, the system further comprising:

a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the first processed information generated by the integrated circuit instruction execution circuit.

--141. An integrated circuit digital signal processor implemented on a single integrated circuit chip, the integrated circuit digital signal processor comprising:

an integrated circuit operand memory storing computer operands, the integrated circuit operand memory implemented on the single integrated circuit chip;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory, the integrated circuit operand memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory storing a computer program comprising computer instructions and storing an interrupt program comprising interrupt instructions, the integrated circuit read only memory implemented on the single integrated circuit chip;

an integrated circuit read only memory address circuit generating instruction addresses, the integrated circuit read only memory address circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed

computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt input circuit generating input interrupt information, the integrated circuit interrupt input circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt execution circuit coupled to the integrated circuit instruction execution circuit and coupled to the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit interrupting the generating of the first processed information by the integrated circuit instruction execution circuit in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit implemented on the single integrated circuit chip;

an integrated circuit operand memory writing circuit coupled to the integrated circuit operand memory and coupled to the integrated circuit interrupt input circuit, the integrated circuit operand memory writing circuit writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit operand memory storing the interrupt return instruction address written by the integrated circuit operand memory writing circuit, the integrated circuit operand memory writing circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt address circuit generating an input interrupt address, the integrated circuit interrupt address circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory address circuit further coupled to the integrated circuit interrupt address circuit and generating interrupt instruction addresses in response to the input interrupt address generated by the integrated circuit interrupt address circuit;

the integrated circuit read only memory accessing circuit generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit instruction execution circuit generating interrupt information in response to the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit and generating interrupt return information in response to at least one of the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit operand memory accessing circuit further coupled to the integrated circuit instruction execution circuit and generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information generated by the integrated circuit instruction execution circuit;

the integrated circuit instruction execution circuit further generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit direct transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating direct transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit direct transfer circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information generated by the integrated circuit direct transfer circuit;

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed directly transferred computer instruction generated by the integrated circuit read only memory accessing circuit;

an integrated circuit indirect transfer memory storing an indirect transfer address, the integrated circuit indirect transfer memory implemented on the single integrated circuit chip;

an integrated circuit indirect transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating indirect transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit indirect transfer circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indirect transfer memory and generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information generated by the integrated circuit indirect transfer circuit; and

the integrated circuit instruction execution circuit generating fourth processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indirectly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

--142. A system comprising the integrated circuit digital signal processor as set forth in claim 141, the system further comprising:

a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit.

--143. An integrated circuit digital signal processor implemented on a single integrated circuit chip, the integrated circuit digital signal processor comprising:

an integrated circuit operand memory storing computer operands, the integrated circuit operand memory implemented on the single integrated circuit chip;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory, the integrated circuit operand memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory storing a computer program comprising computer instructions, the integrated circuit read only memory implemented on the single integrated circuit chip;

an integrated circuit read only memory address circuit generating instruction addresses, the integrated circuit read only memory address circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the

integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit implemented on the single integrated circuit chip;

an integrated circuit direct transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating direct transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit direct transfer circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information generated by the integrated circuit direct transfer circuit;

the integrated circuit instruction execution circuit generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed directly transferred computer instruction generated by the integrated circuit read only memory accessing circuit;

an integrated circuit indirect transfer memory storing an indirect transfer address, the integrated circuit indirect transfer memory implemented on the single integrated circuit chip;

an integrated circuit indirect transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating indirect transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit indirect transfer circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indirect transfer memory and generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information generated by the integrated circuit indirect transfer circuit; and

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indirectly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

144. A system comprising the integrated circuit digital signal processor as set forth in claim 143, the system further comprising:

a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit.

--145. An integrated circuit digital signal processor implemented on a single integrated circuit chip, the integrated circuit digital signal processor comprising:

an integrated circuit operand memory storing computer operands, the integrated circuit operand memory implemented on the single integrated circuit chip;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory, the integrated circuit operand memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory storing a computer program comprising computer instructions and storing an interrupt program comprising interrupt instructions, the integrated circuit read only memory implemented on the single integrated circuit chip;

an integrated circuit read only memory address circuit generating instruction addresses, the integrated circuit read only memory address circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the

integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt input circuit generating input interrupt information, the integrated circuit interrupt input circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt execution circuit coupled to the integrated circuit instruction execution circuit and coupled to the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit interrupting the generating of the first processed information by the integrated circuit instruction execution circuit in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit implemented on the single integrated circuit chip;

an integrated circuit operand memory writing circuit coupled to the integrated circuit operand memory and coupled to the integrated circuit interrupt input circuit, the integrated circuit operand memory writing circuit writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit operand memory storing the interrupt return instruction address written by the integrated circuit operand memory writing circuit, the integrated circuit operand memory writing circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt address circuit generating an input interrupt address, the integrated circuit interrupt address circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory address circuit further coupled to the integrated circuit interrupt address circuit and generating interrupt instruction addresses in response to the input interrupt address generated by the integrated circuit interrupt address circuit;

the integrated circuit read only memory accessing circuit generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit instruction execution circuit generating interrupt information in response to the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit and generating interrupt return information in response to at least one of the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit operand memory accessing circuit further coupled to the integrated circuit instruction execution circuit and generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information generated by the integrated circuit instruction execution circuit;

the integrated circuit instruction execution circuit further generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit indirect transfer memory storing an indirect transfer address, the integrated circuit indirect transfer memory implemented on the single integrated circuit chip;

an integrated circuit indirect transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating indirect transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit indirect transfer circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indirect transfer memory and generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information generated by the integrated circuit indirect transfer circuit; and

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indirectly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

147-146. A system comprising the integrated circuit digital signal processor as set forth in claim 145, the system further comprising:

a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller.

--147. An integrated circuit digital signal processor implemented on a single integrated circuit chip, the integrated circuit digital signal processor comprising:

an integrated circuit operand memory storing computer operands, the integrated circuit operand memory implemented on the single integrated circuit chip;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory, the integrated circuit operand memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory storing a computer program comprising computer instructions and storing an interrupt program comprising interrupt instructions, the integrated circuit read only memory implemented on the single integrated circuit chip;

an integrated circuit read only memory address circuit generating instruction addresses, the integrated circuit read only memory address circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the

integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt input circuit generating input interrupt information, the integrated circuit interrupt input circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt execution circuit coupled to the integrated circuit instruction execution circuit and coupled to the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit interrupting the generating of the first processed information by the integrated circuit instruction execution circuit in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit implemented on the single integrated circuit chip;

an integrated circuit operand memory writing circuit coupled to the integrated circuit operand memory and coupled to the integrated circuit interrupt input circuit, the integrated circuit operand memory writing circuit writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit operand memory storing the interrupt return instruction address written by the integrated circuit operand memory writing circuit, the integrated circuit operand memory writing circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt address circuit generating an input interrupt address, the integrated circuit interrupt address circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory address circuit further coupled to the integrated circuit interrupt address circuit and generating interrupt instruction addresses in response to the input interrupt address generated by the integrated circuit interrupt address circuit;

the integrated circuit read only memory accessing circuit generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit instruction execution circuit generating interrupt information in response to the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit and generating interrupt return information in response to at least one of the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit operand memory accessing circuit further coupled to the integrated circuit instruction execution circuit and generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information generated by the integrated circuit instruction execution circuit;

the integrated circuit instruction execution circuit further generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit direct transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating direct transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit direct transfer circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information generated by the integrated circuit direct transfer circuit; and

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed directly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

--148. A system comprising the integrated circuit digital signal processor as set forth in claim 147, the system further comprising:

a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller.

--149. An integrated circuit digital signal processor implemented on a single integrated circuit chip, the integrated circuit digital signal processor comprising:

an integrated circuit operand memory storing computer operands, the integrated circuit operand memory implemented on the single integrated circuit chip;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory, the integrated circuit operand memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory storing a computer program comprising computer instructions and storing an interrupt program comprising interrupt instructions, the integrated circuit read only memory implemented on the single integrated circuit chip;

an integrated circuit read only memory address circuit generating instruction addresses, the integrated circuit read only memory address circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt input circuit generating input interrupt information, the integrated circuit interrupt input circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt execution circuit coupled to the integrated circuit instruction execution circuit and coupled to the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit interrupting the generating of the first processed information by the integrated circuit instruction execution circuit in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit implemented on the single integrated circuit chip;

an integrated circuit operand memory writing circuit coupled to the integrated circuit operand memory and coupled to the integrated circuit interrupt input circuit, the integrated circuit operand memory writing circuit writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit operand memory storing the interrupt return instruction address written by the integrated circuit operand memory writing circuit, the integrated circuit operand memory writing circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt address circuit generating an input interrupt address, the integrated circuit interrupt address circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory address circuit further coupled to the integrated circuit interrupt address circuit and generating interrupt instruction addresses in response to the input interrupt address generated by the integrated circuit interrupt address circuit;

the integrated circuit read only memory accessing circuit generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit instruction execution circuit generating interrupt information in response to the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit and generating interrupt return information in response to at least one of the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit operand memory accessing circuit further coupled to the integrated circuit instruction execution circuit and generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information generated by the integrated circuit instruction execution circuit;

the integrated circuit instruction execution circuit further generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit index memory storing an index operand, the integrated circuit index memory implemented on the single integrated circuit chip;

an integrated circuit indexing circuit coupled to the integrated circuit read only memory address circuit and coupled to the integrated circuit index memory, the integrated circuit indexing circuit generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses generated by the integrated circuit read only memory address circuit, the integrated circuit indexing circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indexing circuit and generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address generated by the integrated circuit indexing circuit;

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indexed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit direct transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating direct transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit direct transfer circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information generated by the integrated circuit direct transfer circuit;

the integrated circuit instruction execution circuit generating fourth processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed directly transferred computer instruction generated by the integrated circuit read only memory accessing circuit;

an integrated circuit indirect transfer memory storing an indirect transfer address, the integrated circuit indirect transfer memory implemented on the single integrated circuit chip;

an integrated circuit indirect transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating indirect transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit indirect transfer circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indirect transfer memory and generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information generated by the integrated circuit indirect transfer circuit; and

the integrated circuit instruction execution circuit generating fifth processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indirectly transferred computer instruction generated by the integrated circuit read only memory accessing circuit.

--150. An integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 149, the integrated circuit instruction execution circuit comprising:

an input circuit generating input information;

a frame loop heading circuit generating frame loop heading information;

a frame loop initializing circuit initializing frame loop information in response to the frame loop heading information;

a frame loop looping circuit looping through a frame loop in response to the frame loop information;

a frame loop update circuit updating the frame loop information in response to the looping through the frame loop;

a block loop heading circuit generating block loop heading information;

a block loop initializing circuit initializing block loop information in response to the block loop heading information and in response to the looping through the frame loop;

a block loop looping circuit looping through a block loop in response to the block loop information;

a block loop update circuit updating the block loop information in response to the looping through the block loop;

a sample loop heading circuit generating sample loop heading information;

a sample loop initializing circuit initializing sample loop information in response to the sample loop heading information and in response to the looping through the block loop;

a sample loop looping circuit looping through a sample loop in response to the sample loop information;

a sample loop update circuit updating the sample loop information in response to the looping through the sample loop;

a first output circuit generating change information in response to the input information and in response to the looping through the sample loop; and

a second output circuit generating output rounded off change information in response to the change information.

--151. A system comprising the integrated circuit digital signal processor as set forth in claim 149, the system further comprising:

a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller.

--152. A system comprising the integrated circuit digital signal processor as set forth in claim 149, the system further comprising:

a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the first processed information generated by the integrated circuit instruction execution circuit.

--153. A system comprising the integrated circuit digital signal processor as set forth in claim 149, the system further comprising:

a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit.

--154. A system comprising the integrated circuit digital signal processor as set forth in claim 149, the system further comprising:

a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit.

--155. An integrated circuit digital signal processor implemented on a single integrated circuit chip, the integrated circuit digital signal processor comprising:

an integrated circuit operand memory storing computer operands, the integrated circuit operand memory implemented on the single integrated circuit chip;

an integrated circuit operand memory accessing circuit coupled to the integrated circuit operand memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory, the integrated circuit operand memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory storing a computer program comprising computer instructions and storing an interrupt program comprising interrupt instructions, the integrated circuit read only memory implemented on the single integrated circuit chip;

an integrated circuit read only memory address circuit generating instruction addresses, the integrated circuit read only memory address circuit implemented on the single integrated circuit chip;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and coupled to the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses generated by the integrated circuit read only memory address circuit, the integrated circuit read only memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit instruction execution circuit coupled to the integrated circuit operand memory accessing circuit and coupled to the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit generating first processed information in response to the accessed computer operands generated by the

integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit instruction execution circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt input circuit generating input interrupt information, the integrated circuit interrupt input circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt execution circuit coupled to the integrated circuit instruction execution circuit and coupled to the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit interrupting the generating of the first processed information by the integrated circuit instruction execution circuit in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit implemented on the single integrated circuit chip;

an integrated circuit operand memory writing circuit coupled to the integrated circuit operand memory and coupled to the integrated circuit interrupt input circuit, the integrated circuit operand memory writing circuit writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information generated by the integrated circuit interrupt input circuit, the integrated circuit operand memory storing the interrupt return instruction address written by the integrated circuit operand memory writing circuit, the integrated circuit operand memory writing circuit implemented on the single integrated circuit chip;

an integrated circuit interrupt address circuit generating an input interrupt address, the integrated circuit interrupt address circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory address circuit further coupled to the integrated circuit interrupt address circuit and generating interrupt instruction addresses in response to the input interrupt address generated by the integrated circuit interrupt address circuit;

the integrated circuit read only memory accessing circuit generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses generated by the integrated circuit read only memory address circuit;

the integrated circuit instruction execution circuit generating interrupt information in response to the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit and generating interrupt return information in response to at least one of the accessed interrupt instructions generated by the integrated circuit read only memory accessing circuit;

the integrated circuit operand memory accessing circuit further coupled to the integrated circuit instruction execution circuit and generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information generated by the integrated circuit instruction execution circuit;

the integrated circuit instruction execution circuit further generating second processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit index memory storing an index operand, the integrated circuit index memory implemented on the single integrated circuit chip;

an integrated circuit indexing circuit coupled to the integrated circuit read only memory address circuit and coupled to the integrated circuit index memory, the integrated circuit indexing circuit generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses generated by the integrated circuit read only memory address circuit, the integrated circuit indexing circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indexing circuit and generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address generated by the integrated circuit indexing circuit;

the integrated circuit instruction execution circuit generating third processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indexed computer instructions generated by the integrated circuit read only memory accessing circuit;

an integrated circuit direct transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating direct transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit direct transfer circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information generated by the integrated circuit direct transfer circuit;

the integrated circuit instruction execution circuit generating fourth processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed directly transferred computer instruction generated by the integrated circuit read only memory accessing circuit;

an integrated circuit indirect transfer memory storing an indirect transfer address, the integrated circuit indirect transfer memory implemented on the single integrated circuit chip;

an integrated circuit indirect transfer circuit coupled to the integrated circuit read only memory accessing circuit and generating indirect transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, the integrated circuit indirect transfer circuit implemented on the single integrated circuit chip;

the integrated circuit read only memory accessing circuit further coupled to the integrated circuit indirect transfer memory and generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information generated by the integrated circuit indirect transfer circuit; and

the integrated circuit instruction execution circuit generating fifth processed information in response to the accessed computer operands generated by the integrated circuit operand memory accessing circuit and in response to the accessed indirectly transferred computer instruction generated by the integrated circuit read only memory accessing circuit;

the integrated circuit instruction execution circuit comprising:

an input circuit generating input information,

an outer loop header circuit generating outer loop header information,

an outer loop initializing circuit initializing outer loop information in response to the outer loop header information,

an outer loop looping circuit looping through an outer loop in response to the outer loop information,

an outer loop update circuit updating the outer loop information in response to the looping through the outer loop,

an outer loop exiting circuit exiting the outer loop in response to the outer loop information,

a middle loop header circuit generating middle loop header information,

a middle loop initializing circuit initializing middle loop information in response to the middle loop header information and in response to the looping through the outer loop,

a middle loop looping circuit looping through a middle loop in response to the middle loop information,

a middle loop update circuit updating the middle loop information in response to the looping through the middle loop,

a middle loop exiting circuit exiting the middle loop in response to the middle loop information,

an inner loop header circuit generating inner loop header information,

an inner loop initializing circuit initializing inner loop information in response to the inner loop header information and in response to the looping through the middle loop,

an inner loop looping circuit looping through an inner loop in response to the inner loop information,

a skipping circuit skipping at least one loop through the inner loop in response to the inner loop information,

an inner loop update circuit updating the inner loop information in response to the looping through the inner loop,

a first output circuit generating product information in response to the input information and in response to the looping through the inner loop,

a second output circuit generating output rounded off product information in response to the product information, and

an inner loop exiting circuit exiting the inner loop in response to the inner loop information.

--156. A system comprising the integrated circuit digital signal processor as set forth in claim 155, the system further comprising:

a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller.

--157. A system comprising the integrated circuit digital signal processor as set forth in claim 155, the system further comprising:

a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the first processed information generated by the integrated circuit instruction execution circuit.

--158. A system comprising the integrated circuit digital signal processor as set forth in claim 155, the system further comprising:

a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit.

--159. A system comprising the integrated circuit digital signal processor as set forth in claim 155, the system further comprising:

a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit.

--160. An integrated circuit digital signal processor system comprising:

a keyboard circuit generating keyboard information;

a serial keyboard communication channel coupled to the keyboard circuit and communicating serial keyboard information in response to the keyboard information generated by the keyboard circuit;

an integrated circuit read only memory storing computer instructions, the integrated circuit read only memory implemented on a single integrated circuit chip;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory, the integrated circuit read only memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing computer operands, the integrated circuit alterable memory implemented on the single integrated circuit chip;

an integrated circuit alterable memory accessing circuit coupled to the integrated circuit alterable memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit alterable memory, the integrated circuit alterable memory accessing circuit implemented on the single integrated circuit chip;

an integrated circuit data processor coupled to the serial keyboard communication channel, coupled to the integrated circuit read only memory accessing circuit, and coupled to the integrated circuit alterable memory accessing circuit, the integrated circuit data processor generating processed information in response to the serial keyboard information communicated by the serial keyboard communication channel, in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, and in response to the accessed computer operands generated by the integrated circuit alterable memory accessing circuit, the integrated circuit data processor implemented on the single integrated circuit chip; and

an integrated circuit memory input circuit coupled to the integrated circuit data processor, coupled to the integrated circuit read only memory accessing circuit, and coupled to the integrated circuit alterable memory, the integrated circuit memory input circuit inputting processed computer operands into the integrated circuit alterable memory in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit and in response to the processed information generated by the

integrated circuit data processor, the integrated circuit alterable memory storing the processed computer operands input by the integrated circuit memory input circuit, the integrated circuit memory input circuit implemented on the single integrated circuit chip.

--161. An integrated circuit digital signal processor system as set forth in claim 160, further comprising:

a serial display communication channel coupled to the integrated circuit data processor and communicating serial display information in response to the processed information generated by the integrated circuit data processor; and

a display device coupled to the serial display communication channel and displaying machine information in response to the serial display information communicated by the serial display communication channel.

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#24

--162. An integrated circuit digital signal processor system as set forth in claim 160, further comprising:

a serial communication channel coupled to the integrated circuit data processor and communicating first serial machine information, second serial machine information, and third serial machine information in response to the processed information generated by the integrated circuit data processor;

a first machine register;

a first machine register input circuit coupled to the serial communication channel and coupled to the first machine register, the first machine register input circuit inputting first input machine information into the first machine register in response to the first serial machine information communicated by the serial communication channel, the first machine register storing the first input machine information input by the first machine register input circuit;

a first machine circuit coupled to the first machine register and generating first output machine information in response to the first input machine information stored in the first machine register;

a first machine element coupled to the first machine circuit and performing a first machine operation in response to the first output machine information generated by the first machine circuit;

a second machine register;

a second machine register input circuit coupled to the serial communication channel and coupled to the second machine register, the second machine register input circuit inputting second input machine information into the second machine register in response to the second serial machine information communicated by the serial communication channel, the second machine register storing the second input machine information input by the second machine register input circuit;

a second machine circuit coupled to the second machine register and generating second output machine information in response to the second input machine information stored in the second machine register;

a second machine element coupled to the second machine circuit and performing a second machine operation in response to the second output machine information generated by the second machine circuit;

a third machine register;

a third machine register input circuit coupled to the serial communication channel and coupled to the third machine register, the third machine register input circuit inputting third input machine information into the third machine register in response to the third serial machine information communicated by the serial communication channel, the third machine register storing the third input machine information input by the third machine register input circuit;

a third machine circuit coupled to the third machine register and generating third output machine information in response to the third input machine information stored in the third machine register; and

a third machine element coupled to the third machine circuit and performing a third machine operation in response to the third output machine information generated by the third machine circuit.

--163. An integrated circuit digital signal processor system as set forth in claim 160, further comprising:

a serial communication link coupled to the integrated circuit data processor and communicating serial information in response to the processed information generated by the integrated circuit data processor;

a storing circuit coupled to the serial communication link and storing output machine information in response to the serial output information communicated by the serial communication link; and

a machine circuit coupled to the storing circuit and generating machine information in response to the output machine information stored in the storing circuit.

--164. An integrated circuit digital signal processor system as set forth in claim 160, wherein the integrated circuit data processor is a monolithic integrated circuit data processor, the monolithic integrated circuit data processor including a monolithic integrated circuit alterable memory and a monolithic integrated circuit read only memory.

--165. A digital signal processor system comprising:

a keyboard circuit generating keyboard information;

a serial keyboard communication channel coupled to the keyboard circuit and communicating serial keyboard information in response to the keyboard information generated by the keyboard circuit;

an integrated circuit read only memory storing computer instructions;

an integrated circuit read only memory accessing circuit coupled to the integrated circuit read only memory and generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory;

an integrated circuit alterable memory storing computer operands;

an integrated circuit alterable memory accessing circuit coupled to the integrated circuit alterable memory and generating accessed computer operands in response to the computer operands stored in the integrated circuit alterable memory;

an integrated circuit data processor coupled to the serial keyboard communication channel, coupled to the machine feedback circuit, coupled to the integrated circuit read only memory accessing circuit, and coupled to the integrated circuit alterable memory accessing circuit, the integrated circuit data processor generating processed information in response to the serial keyboard information communicated by the serial keyboard communication channel, in response to the machine feedback information generated by the machine feedback circuit, in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit, and in response to the accessed computer operands generated by the integrated circuit alterable memory accessing circuit; and

an integrated circuit memory input circuit coupled to the integrated circuit data processor, coupled to the integrated circuit read only memory accessing circuit, and coupled to the integrated circuit alterable memory, the integrated circuit memory input circuit

inputting processed computer operands into the integrated circuit alterable memory in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit and in response to the processed information generated by the integrated circuit data processor, the integrated circuit alterable memory storing the processed computer operands input by the integrated circuit memory input circuit.

--166. A digital signal processor system as set forth in claim 165, further comprising:

a serial display communication channel coupled to the integrated circuit data processor and communicating serial display information in response to the processed information generated by the integrated circuit data processor; and

a display device coupled to the serial display communication channel and displaying machine information in response to the serial display information communicated by the serial display communication channel.

--167. A digital signal processor system as set forth in claim 165, further comprising:

a serial communication channel coupled to the integrated circuit data processor and communicating first serial machine information, second serial machine information, and third serial machine information in response to the processed information generated by the integrated circuit data processor;

a first machine register;

a first machine register input circuit coupled to the serial communication channel and coupled to the first machine register, the first machine register input circuit inputting first input machine information into the first machine register in response to the first serial machine information communicated by the serial communication channel, the first machine register storing the first input machine information input by the first machine register input circuit;

a first machine circuit coupled to the first machine register and generating first output machine information in response to the first input machine information stored in the first machine register;

a first machine element coupled to the first machine circuit and performing a first machine operation in response to the first output machine information generated by the first machine circuit;

a second machine register;

a second machine register input circuit coupled to the serial communication channel and coupled to the second machine register, the second machine register input circuit inputting second input machine information into the second machine register in response to the second serial machine information communicated by the serial communication channel, the second machine register storing the second input machine information input by the second machine register input circuit;

a second machine circuit coupled to the second machine register and generating second output machine information in response to the second input machine information stored in the second machine register;

a second machine element coupled to the second machine circuit and performing a second machine operation in response to the second output machine information generated by the second machine circuit;

a third machine register;

a third machine register input circuit coupled to the serial communication channel and coupled to the third machine register, the third machine register input circuit inputting third input machine information into the third machine register in response to the third serial machine information communicated by the serial communication channel, the third machine register storing the third input machine information input by the third machine register input circuit;

a third machine circuit coupled to the third machine register and generating third output machine information in response to the third input machine information stored in the third machine register; and

a third machine element coupled to the third machine circuit and performing a third machine operation in response to the third output machine information generated by the third machine circuit.

--168. A digital signal processor system as set forth in claim 165, further comprising:

a serial communication link coupled to the integrated circuit data processor and communicating serial information in response to the processed information generated by the integrated circuit data processor;

a storing circuit coupled to the serial communication link and storing output machine information in response to the serial output information communicated by the serial communication link; and

a machine circuit coupled to the storing circuit and generating machine information in response to the output machine information stored in the storing circuit.

--169. A digital signal processor system as set forth in claim 165, wherein the integrated circuit data processor is implemented on a single integrated circuit chip.

--170. A digital signal processor system as set forth in claim 165, wherein the integrated circuit data processor is a monolithic integrated circuit data processor, the monolithic integrated circuit data processor including a monolithic integrated circuit alterable memory and a monolithic integrated circuit read only memory.

--171. A digital signal processor system comprising:

a machine data processor implemented on a single integrated circuit chip.

--172. A digital signal processor system comprising:

a data processor implemented on a single integrated circuit chip.

--173. A digital signal processor system as set forth in claim 172, further comprising:

a read only memory implemented on the single integrated circuit chip; and

an alterable memory implemented on the single integrated circuit chip.

--174. A digital signal processor system as set forth in claim 172, further comprising:

a photo optical machine coupled to the data processor implemented on the single integrated circuit chip, the photo optical machine generating a photo optical mask in response to data processed by the data processor.

--175. A digital signal processor system as set forth in claim 172, further comprising:

a pattern generator coupled to the data processor implemented on the single integrated circuit chip, the pattern generator generating a pattern in response to data processed by the data processor.

--176. A digital signal processor system as set forth in claim 172, further comprising:

a plotter coupled to the data processor implemented on the single integrated circuit chip, the plotter generating a plot in response to data processed by the data processor.

--177. A digital signal processor system comprising:

a read only memory implemented on a single integrated circuit chip; and

an alterable memory implemented on the single integrated circuit chip

--178. A process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip, the process comprising the acts of:

storing computer operands in an integrated circuit operand memory, the integrated circuit operand memory implemented on the single integrated circuit chip;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory, the integrated circuit read only memory implemented on the single integrated circuit chip;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses; and

generating processed information in response to the accessed computer operands and in response to the accessed computer instructions.

--179. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 178, the process further comprising the acts of:

generating machine control information in response to the processed information; and

operating a machine in response to the machine control information.

--180. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 178, the process further comprising the act of communicating information to a remote location in response to the processed information.

--181. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 178, the process further comprising the acts of:

generating display information in response to the processed information; and

displaying information in response to the display information.

--182. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 178, the process further comprising the acts of:

generating graphics information in response to the processed information; and

displaying graphics images in response to the graphics information.

--183. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 178, the act of generating the processed information comprising the acts of:

generating input information;

generating loop header information;

initializing loop information in response to the loop header information;

looping through a loop in response to the loop information;

skipping at least one loop through the loop in response to the loop information;

updating the loop information in response to the looping through the loop;

generating product information in response to the input information and in response to the looping through the loop; and

generating output rounded off product information in response to the product information.

--184. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 178, the process further comprising the act of making a product in response to the processed information.

--185. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 178, the process further comprising the act of making a communication product in response to the processed information.

--186. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 178, the process further comprising the act of making a designed product in response to the processed information.

--187. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 178, the process further comprising the act of making an electric product in response to the processed information.

--188. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 178, the process further comprising the act of making a disk memory product in response to the processed information.

--189. A process of operating a digital signal processor comprising the acts of:

storing computer operands in an integrated circuit operand memory;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses; and

generating processed information in response to the accessed computer operands and in response to the accessed computer instructions.

--190. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 189, the process further comprising the acts of:

generating machine control information in response to the processed information; and

operating a machine in response to the machine control information.

--191. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 189, the process further comprising the act of communicating information to a remote location in response to the processed information.

--192. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 189, the process further comprising the acts of:

generating display information in response to the processed information; and

displaying information in response to the display information.

--193. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 189, the process further comprising the acts of:

generating graphics information in response to the processed information; and

displaying graphics images in response to the graphics information.

--194. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 189, the act of generating the processed information comprising the acts of:

generating input information;

generating synchronization information;

generating outer loop header information;

initializing outer loop information in response to the outer loop header information and in response to the synchronization information;

looping through an outer loop in response to the outer loop information;

updating the outer loop information in response to the looping through the outer loop;

exiting the outer loop in response to the outer loop information;

generating middle loop header information;

initializing middle loop information in response to the middle loop header information and in response to the looping through the outer loop;

looping through a middle loop in response to the middle loop information;

updating the middle loop information in response to the looping through the middle loop;

exiting the middle loop in response to the middle loop information;

generating inner loop header information;

initializing inner loop information in response to the inner loop header information and in response to the looping through the middle loop;

looping through an inner loop in response to the inner loop information;

skipping at least one loop through the inner loop in response to the inner loop information;

updating the inner loop information in response to the looping through the inner loop;

generating change information in response to the input information and in response to the looping through the inner loop;

generating output rounded off change information in response to the change information; and

exiting the inner loop in response to the inner loop information.

--195. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 189, the process further comprising the act of making a product in response to the processed information.

--196. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 189, the process further comprising the act of making a photo electric product in response to the processed information.

--197. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 189, the process further comprising the act of making a process control product in response to the processed information.

--198. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 189, the process further comprising the act of making a brake product in response to the processed information.

--199. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 189, the process further comprising the act of making a servo control product in response to the processed information.

--200. A process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip, the process comprising the acts of:

storing computer operands in an integrated circuit operand memory, the integrated circuit operand memory implemented on the single integrated circuit chip;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory and storing an interrupt program comprising interrupt instructions in the integrated circuit read only memory, the integrated circuit read only memory implemented on the single integrated circuit chip;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating input interrupt information;

interrupting the generating of the first processed information in response to the input interrupt information;

writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information, the integrated circuit operand memory storing the interrupt return instruction address;

generating an input interrupt address;

generating interrupt instruction addresses in response to the input interrupt address;

generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses;

generating interrupt information in response to the accessed interrupt instructions and generating interrupt return information in response to at least one of the accessed interrupt instructions;

generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information; and

generating second processed information in response to the accessed computer operands and in response to the accessed computer instructions.

--201. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 200, the process further comprising the acts of:

generating machine control information in response to the first processed information; and

operating a machine in response to the machine control information.

--202. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 200, the process further comprising the act of making a product in response to the second processed information.

--203. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 200, the process further comprising the act of making a location product in response to the second processed information.

--204. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 200, the process further comprising the act of making a processed product in response to the second processed information.

--205. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 200, the process further comprising the act of making a photo product in response to the second processed information.

--206. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 200, the process further comprising the act of making a velocity control product in response to the second processed information.

--207. A process of operating a digital signal processor comprising the acts of:

storing computer operands in an integrated circuit operand memory;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

storing an index operand in an integrated circuit index memory;

generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses;

generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address; and

generating second processed information in response to the accessed computer operands and in response to the accessed indexed computer instructions.

--208. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 207, the process further comprising the act of communicating information to a remote location in response to the first processed information.

--209. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 207, the process further comprising the act of making a product in response to the first processed information.

--210. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 207, the process further comprising the act of making a printed product in response to the first processed information.

--211. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 207, the process further comprising the act of making a graphics product in response to the first processed information.

--212. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 207, the process further comprising the act of making a payroll product in response to the first processed information.

--213. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 207, the process further comprising the act of making a business product in response to the first processed information.

--214. A process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip, the process comprising the acts of:

storing computer operands in an integrated circuit operand memory, the integrated circuit operand memory implemented on the single integrated circuit chip;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory, the integrated circuit read only memory implemented on the single integrated circuit chip;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating direct transfer information in response to the accessed computer instructions;

generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information; and

generating second processed information in response to the accessed computer operands and in response to the accessed directly transferred computer instruction.

--215. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 214, the process further comprising the acts of:

generating display information in response to the first processed information; and

displaying information in response to the display information.

--216. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 214, the process further comprising the act of making a product in response to the second processed information.

--217. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 214, the process further comprising the act of making a communicated product in response to the second processed information.

--218. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 214, the process further comprising the act of making an inventoried product in response to the second processed information.

--219. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 214, the process further comprising the act of making an accounted product in response to the second processed information.

--220. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 214, the process further comprising the act of making an electric product in response to the second processed information.

--221. A process of operating a digital signal processor comprising the acts of:

storing computer operands in an integrated circuit operand memory;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

storing an indirect transfer address in an integrated circuit indirect transfer memory;

generating indirect transfer information in response to the accessed computer instructions;

generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information; and

generating second processed information in response to the accessed computer operands and in response to the accessed indirectly transferred computer instruction.

--222. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 221, the process further comprising the acts of:

generating graphics information in response to the first processed information; and

displaying graphics images in response to the graphics information.

--223. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 221, the process further comprising the act of making a product in response to the first processed information.

--224. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 221, the process further comprising the act of making a signal product in response to the first processed information.

--225. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 221, the process further comprising the act of making a natural resource product in response to the first processed information.

--226. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 221, the process further comprising the act of making a telephone product in response to the first processed information.

--227. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 221, the process further comprising the act of making an acceleration control product in response to the first processed information.

--228. A process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip, the process comprising the acts of:

storing computer operands in an integrated circuit operand memory, the integrated circuit operand memory implemented on the single integrated circuit chip;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory and storing an interrupt program comprising interrupt instructions in the integrated circuit read only memory, the integrated circuit read only memory implemented on the single integrated circuit chip;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating input interrupt information;

interrupting the generating of the first processed information in response to the input interrupt information;

writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information, the integrated circuit operand memory storing the interrupt return instruction address;

generating an input interrupt address;

generating interrupt instruction addresses in response to the input interrupt address;

generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses;

generating interrupt information in response to the accessed interrupt instructions and generating interrupt return information in response to at least one of the accessed interrupt instructions;

generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information;

generating second processed information in response to the accessed computer operands and in response to the accessed computer instructions;

storing an index operand in an integrated circuit index memory, the integrated circuit index memory implemented on the single integrated circuit chip;

generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses;

generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address; and

generating third processed information in response to the accessed computer operands and in response to the accessed indexed computer instructions.

--229. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 228, the process further comprising the acts of:

generating machine control information in response to the first processed information; and

operating a machine in response to the machine control information.

--230. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 228, the process further comprising the act of making a product in response to the third processed information.

--231. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 228, the process further comprising the act of making a machine product in response to the third processed information.

--232. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 228, the process further comprising the act of making a plotter product in response to the third processed information.

--233. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 228, the process further comprising the act of making a data processed product in response to the third processed information.

--234. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 228, the process further comprising the act of making a mineral product in response to the third processed information.

--235. A process of operating a digital signal processor comprising the acts of:

storing computer operands in an integrated circuit operand memory;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory and storing an interrupt program comprising interrupt instructions in the integrated circuit read only memory;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating input interrupt information;

interrupting the generating of the first processed information in response to the input interrupt information;

writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information, the integrated circuit operand memory storing the interrupt return instruction address;

generating an input interrupt address;

generating interrupt instruction addresses in response to the input interrupt address;

generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses;

generating interrupt information in response to the accessed interrupt instructions and generating interrupt return information in response to at least one of the accessed interrupt instructions;

generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information;

generating second processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating direct transfer information in response to the accessed computer instructions;

generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information;

generating third processed information in response to the accessed computer operands and in response to the accessed directly transferred computer instruction;

storing an indirect transfer address in an integrated circuit indirect transfer memory;

generating indirect transfer information in response to the accessed computer instructions;

generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information; and

generating fourth processed information in response to the accessed computer operands and in response to the accessed indirectly transferred computer instruction.

F24 #1

--236. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 235, the process further comprising the act of communicating information to a remote location in response to the first processed information.

--237. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 235, the process further comprising the act of making a product in response to the first processed information.

--238. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 235, the process further comprising the act of making an inventory product in response to the first processed information.

--239. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 235, the process further comprising the act of making a printer product in response to the first processed information.

--240. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 235, the process further comprising the act of making a process product in response to the first processed information.

--241. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 235, the process further comprising the act of making a moving product in response to the first processed information.

--242. A process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip, the process comprising the acts of:

storing computer operands in an integrated circuit operand memory, the integrated circuit operand memory implemented on the single integrated circuit chip;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory, the integrated circuit read only memory implemented on the single integrated circuit chip;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

storing an index operand in an integrated circuit index memory, the integrated circuit index memory implemented on the single integrated circuit chip;

generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses;

generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address;

generating second processed information in response to the accessed computer operands and in response to the accessed indexed computer instructions;

generating direct transfer information in response to the accessed computer instructions;

generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information;

generating third processed information in response to the accessed computer operands and in response to the accessed directly transferred computer instruction;

storing an indirect transfer address in an integrated circuit indirect transfer memory, the integrated circuit indirect transfer memory implemented on the single integrated circuit chip;

generating indirect transfer information in response to the accessed computer instructions;

generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information; and

generating fourth processed information in response to the accessed computer operands and in response to the accessed indirectly transferred computer instruction.

--243. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 242, the process further comprising the acts of:

generating display information in response to the first processed information; and

displaying information in response to the display information.

--244. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 242, the process further comprising the act of making a product in response to the first processed information.

--245. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 242, the process further comprising the act of making a position control product in response to the first processed information.

--246. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 242, the process further comprising the act of making an oil product in response to the first processed information.

--247. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 242, the process further comprising the act of making an intensity product in response to the first processed information.

--248. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 242, the process further comprising the act of making a turret product in response to the first processed information.

--249. A process of operating a digital signal processor comprising the acts of:

storing computer operands in an integrated circuit operand memory;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating direct transfer information in response to the accessed computer instructions;

generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information;

generating second processed information in response to the accessed computer operands and in response to the accessed directly transferred computer instruction;

storing an indirect transfer address in an integrated circuit indirect transfer memory;

generating indirect transfer information in response to the accessed computer instructions;

generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information; and

generating third processed information in response to the accessed computer operands and in response to the accessed indirectly transferred computer instruction.

--250. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 249, the process further comprising the acts of:

generating graphics information in response to the first processed information; and

displaying graphics images in response to the graphics information.

--251. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 249, the process further comprising the act of making a product in response to the third processed information.

--252. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 249, the process further comprising the act of making an information product in response to the third processed information.

--253. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 249, the process further comprising the act of making a motion control product in response to the third processed information.

--254. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 249, the process further comprising the act of making a plotted product in response to the third processed information.

--255. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 249, the process further comprising the act of making a optical product in response to the third processed information.

--256. A process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip, the process comprising the acts of:

storing computer operands in an integrated circuit operand memory, the integrated circuit operand memory implemented on the single integrated circuit chip;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory, the integrated circuit read only memory implemented on the single integrated circuit chip;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

storing an index operand in an integrated circuit index memory, the integrated circuit index memory implemented on the single integrated circuit chip;

generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses;

generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address;

generating second processed information in response to the accessed computer operands and in response to the accessed indexed computer instructions;

generating direct transfer information in response to the accessed computer instructions;

generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information;

generating third processed information in response to the accessed computer operands and in response to the accessed directly transferred computer instruction;

--257. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 256, the process further comprising the acts of:

generating machine control information in response to the first processed information; and

operating a machine in response to the machine control information.

--258. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 256, the process further comprising the act of making a product in response to the first processed information.

--259. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 256, the process further comprising the act of making an accounting product in response to the first processed information.

--260. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 256, the process further comprising the act of making a photo optical product in response to the first processed information.

--261. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 256, the process further comprising the act of making a telphoned product in response to the first processed information.

--262. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 256, the process further comprising the act of making a manufactured product in response to the first processed information.

--263. A process of operating a digital signal processor comprising the acts of:

storing computer operands in an integrated circuit operand memory;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory and storing an interrupt program comprising interrupt instructions in the integrated circuit read only memory;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating input interrupt information;

interrupting the generating of the first processed information in response to the input interrupt information;

writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information, the integrated circuit operand memory storing the interrupt return instruction address;

generating an input interrupt address;

generating interrupt instruction addresses in response to the input interrupt address;

generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses;

generating interrupt information in response to the accessed interrupt instructions and generating interrupt return information in response to at least one of the accessed interrupt instructions;

generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information;

generating second processed information in response to the accessed computer operands and in response to the accessed computer instructions;

storing an indirect transfer address in an integrated circuit indirect transfer memory;

generating indirect transfer information in response to the accessed computer instructions;

generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information; and

generating third processed information in response to the accessed computer operands and in response to the accessed indirectly transferred computer instruction.

--264. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 263, the process further comprising the act of communicating information to a remote location in response to the first processed information.

--265. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 263, the process further comprising the act of making a product in response to the third processed information.

--266. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 263, the process further comprising the act of making a milled part product in response to the third processed information.

--267. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 263, the process further comprising the act of making a servo product in response to the third processed information.

--268. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 263, the process further comprising the act of making a brake control product in response to the third processed information.

--269. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 263, the process further comprising the act of making a mineral product in response to the third processed information.

--270. A process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip, the process comprising the acts of:

storing computer operands in an integrated circuit operand memory, the integrated circuit operand memory implemented on the single integrated circuit chip;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory, the integrated circuit read only memory implemented on the single integrated circuit chip;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

storing an index operand in an integrated circuit index memory, the integrated circuit index memory implemented on the single integrated circuit chip;

generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses;

generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address;

generating second processed information in response to the accessed computer operands and in response to the accessed indexed computer instructions;

storing an indirect transfer address in an integrated circuit indirect transfer memory, the integrated circuit indirect transfer memory implemented on the single integrated circuit chip;

generating indirect transfer information in response to the accessed computer instructions;

generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information; and

generating third processed information in response to the accessed computer operands and in response to the accessed indirectly transferred computer instruction.

--271. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 270, the process further comprising the acts of:

generating display information in response to the first processed information; and

displaying information in response to the display information.

--272. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 270, the process further comprising the act of making a product in response to the first processed information.

--273. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 270, the process further comprising the act of making a fabricated product in response to the first processed information.

--274. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 270, the process further comprising the act of making an intensity control product in response to the first processed information.

--275. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 270, the process further comprising the act of making a positioned product in response to the first processed information.

--276. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 270, the process further comprising the act of making a velocity product in response to the first processed information.

--277. A process of operating a digital signal processor comprising the acts of:

storing computer operands in an integrated circuit operand memory;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory and storing an interrupt program comprising interrupt instructions in the integrated circuit read only memory;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating input interrupt information;

interrupting the generating of the first processed information in response to the input interrupt information;

writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information, the integrated circuit operand memory storing the interrupt return instruction address;

generating an input interrupt address;

generating interrupt instruction addresses in response to the input interrupt address;

generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses;

generating interrupt information in response to the accessed interrupt instructions and generating interrupt return information in response to at least one of the accessed interrupt instructions;

generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information;

generating second processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating direct transfer information in response to the accessed computer instructions;

generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information; and

generating third processed information in response to the accessed computer operands and in response to the accessed directly transferred computer instruction.

--278. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 277, the process further comprising the acts of:

generating graphics information in response to the first processed information; and

displaying graphics images in response to the graphics information.

--279. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 277, the process further comprising the act of making a product in response to the third processed information.

--280. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 277, the process further comprising the act of making an acceleration product in response to the third processed information.

--281. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 277, the process further comprising the act of making a patterned pattern product in response to the third processed information.

--282. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 277, the process further comprising the act of making a product in response to the third processed information.

--283. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 277, the process further comprising the act of making a position product in response to the third processed information.

--284. A process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip, the process comprising the acts of:

storing computer operands in an integrated circuit operand memory, the integrated circuit operand memory implemented on the single integrated circuit chip;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory and storing an interrupt program comprising interrupt instructions in the integrated circuit read only memory, the integrated circuit read only memory implemented on the single integrated circuit chip;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating input interrupt information;

interrupting the generating of the first processed information in response to the input interrupt information;

writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information, the integrated circuit operand memory storing the interrupt return instruction address;

generating an input interrupt address;

generating interrupt instruction addresses in response to the input interrupt address;

generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses;

generating interrupt information in response to the accessed interrupt instructions and generating interrupt return information in response to at least one of the accessed interrupt instructions;

generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information;

generating second processed information in response to the accessed computer operands and in response to the accessed computer instructions;

storing an index operand in an integrated circuit index memory, the integrated circuit index memory implemented on the single integrated circuit chip;

generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses;

generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address;

generating third processed information in response to the accessed computer operands and in response to the accessed indexed computer instructions;

generating direct transfer information in response to the accessed computer instructions;

generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information; and

generating fourth processed information in response to the accessed computer operands and in response to the accessed directly transferred computer instruction.

--285. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 284, the process further comprising the acts of:

generating machine control information in response to the first processed information; and

operating a machine in response to the machine control information.

--286. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 284, the process further comprising the act of making a product in response to the fourth processed information.

--287. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 284, the process further comprising the act of making a machined part product in response to the fourth processed information.

--288. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 284, the process further comprising the act of making a data processing product in response to the fourth processed information.

--289. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 284, the process further comprising the act of making a service product in response to the fourth processed information.

--290. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 284, the process further comprising the act of making a milling machine product in response to the fourth processed information.

--291. A process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip, the process comprising the acts of:

storing computer operands in an integrated circuit operand memory, the integrated circuit operand memory implemented on the single integrated circuit chip;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory and storing an interrupt program comprising interrupt instructions in the integrated circuit read only memory, the integrated circuit read only memory implemented on the single integrated circuit chip;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating input interrupt information;

interrupting the generating of the first processed information in response to the input interrupt information;

writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information, the integrated circuit operand memory storing the interrupt return instruction address;

generating an input interrupt address;

generating interrupt instruction addresses in response to the input interrupt address;

generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses;

generating interrupt information in response to the accessed interrupt instructions and generating interrupt return information in response to at least one of the accessed interrupt instructions;

generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information;

generating second processed information in response to the accessed computer operands and in response to the accessed computer instructions;

storing an index operand in an integrated circuit index memory, the integrated circuit index memory implemented on the single integrated circuit chip;

generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses;

generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address;

generating third processed information in response to the accessed computer operands and in response to the accessed indexed computer instructions;

storing an indirect transfer address in an integrated circuit indirect transfer memory, the integrated circuit indirect transfer memory implemented on the single integrated circuit chip;

generating indirect transfer information in response to the accessed computer instructions;

generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information; and

generating fourth processed information in response to the accessed computer operands and in response to the accessed indirectly transferred computer instruction.

--292. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 291, the process further comprising the act of communicating information to a remote location in response to the fourth processed information.

--293. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 291, the process further comprising the act of making a product in response to the fourth processed information.

--294. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 291, the process further comprising the act of making a vehicle product in response to the fourth processed information.

--295. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 291, the process further comprising the act of making a machine product in response to the fourth processed information.

--296. A process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip, the process comprising the acts of:

storing computer operands in an integrated circuit operand memory, the integrated circuit operand memory implemented on the single integrated circuit chip;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory and storing an interrupt program comprising interrupt instructions in the integrated circuit read only memory, the integrated circuit read only memory implemented on the single integrated circuit chip;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating input interrupt information;

interrupting the generating of the first processed information in response to the input interrupt information;

writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information, the integrated circuit operand memory storing the interrupt return instruction address;

generating an input interrupt address;

generating interrupt instruction addresses in response to the input interrupt address;

generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses;

generating interrupt information in response to the accessed interrupt instructions and generating interrupt return information in response to at least one of the accessed interrupt instructions;

generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information;

generating second processed information in response to the accessed computer operands and in response to the accessed computer instructions;

storing an index operand in an integrated circuit index memory, the integrated circuit index memory implemented on the single integrated circuit chip;

generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses;

generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address;

generating third processed information in response to the accessed computer operands and in response to the accessed indexed computer instructions;

generating direct transfer information in response to the accessed computer instructions;

generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information;

generating fourth processed information in response to the accessed computer operands and in response to the accessed directly transferred computer instruction;

storing an indirect transfer address in an integrated circuit indirect transfer memory, the integrated circuit indirect transfer memory implemented on the single integrated circuit chip;

generating indirect transfer information in response to the accessed computer instructions;

generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information; and

generating fifth processed information in response to the accessed computer operands and in response to the accessed indirectly transferred computer instruction.

--297. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 296, the process further comprising the acts of:

generating machine control information in response to the first processed information; and

operating a machine in response to the machine control information.

--298. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 296, the process further comprising the act of communicating information to a remote location in response to the first processed information.

--299. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 296, the process further comprising the acts of:

generating display information in response to the first processed information; and

displaying information in response to the display information.

--300. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 296, the process further comprising the acts of:

generating graphics information in response to the first processed information; and

displaying graphics images in response to the graphics information.

--301. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 296, the act of generating the first processed information comprising the acts of:

generating input information;

generating outer loop header information;

initializing outer loop information in response to the outer loop header information;

looping through an outer loop in response to the outer loop information;

generating updated outer loop information in response to the looping through the outer loop;

generating middle loop header information;

initializing middle loop information in response to the middle loop header information and in response to the updated outer loop information;

looping through a middle loop in response to the middle loop information;

generating updated middle loop information in response to the looping through the middle loop;

generating inner loop header information;

initializing inner loop information in response to the inner loop header information and in response to the updated middle loop information;

looping through an inner loop in response to the inner loop information;

skipping at least one loop through the inner loop in response to the inner loop information;

generating updated inner loop information in response to the looping through the inner loop;

generating product information in response to the input information and in response to the updated inner loop information; and

generating output rounded off product information in response to the product information.

--302. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 296, the process further comprising the act of making a product in response to the first processed information.

--303. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 296, the process further comprising the act of making a first product in response to the first processed information.

--304. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 303, the process further comprising the act of making a second product in response to the first product.

--305. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 304, the process further comprising the act of making a third product in response to the second product.

#24
#1

--306. A process of operating a digital signal processor comprising the acts of:

storing computer operands in an integrated circuit operand memory;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory and storing an interrupt program comprising interrupt instructions in the integrated circuit read only memory;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating input interrupt information;

interrupting the generating of the first processed information in response to the input interrupt information;

writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information, the integrated circuit operand memory storing the interrupt return instruction address;

generating an input interrupt address;

generating interrupt instruction addresses in response to the input interrupt address;

generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses;

generating interrupt information in response to the accessed interrupt instructions and generating interrupt return information in response to at least one of the accessed interrupt instructions;

generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information;

generating second processed information in response to the accessed computer operands and in response to the accessed computer instructions;

storing an index operand in an integrated circuit index memory;

generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses;

generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address;

generating third processed information in response to the accessed computer operands and in response to the accessed indexed computer instructions;

generating direct transfer information in response to the accessed computer instructions;

generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information;

generating fourth processed information in response to the accessed computer operands and in response to the accessed directly transferred computer instruction;

storing an indirect transfer address in an integrated circuit indirect transfer memory;

generating indirect transfer information in response to the accessed computer instructions;

generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information; and

generating fifth processed information in response to the accessed computer operands and in response to the accessed indirectly transferred computer instruction.

--307. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 306, the process further comprising the acts of:

generating machine control information in response to the first processed information; and

operating a machine in response to the machine control information.

--308. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 306, the process further comprising the act of communicating information to a remote location in response to the first processed information.

--309. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 306, the process further comprising the acts of:

generating display information in response to the first processed information; and

displaying information in response to the display information.

--310. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 306, the process further comprising the acts of:

generating graphics information in response to the first processed information; and

displaying graphics images in response to the graphics information.

--311. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 306, the act of generating the first processed information comprising the acts of:

generating input information;

generating synchronization information;

generating loop header information;

initializing loop information in response to the loop header information;

looping through a loop in response to the loop information;

generating updated loop information in response to the looping through the loop;

generating change information in response to the input information and in response to the updated loop information; and

generating output rounded off change information in response to the change information.

--312. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 306, the process further comprising the act of making a product in response to the fifth processed information.

--313. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 306, the process further comprising the act of making a data compressed product in response to the fifth processed information.

--314. A process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip, the process comprising the acts of:

storing computer operands in an integrated circuit operand memory, the integrated circuit operand memory implemented on the single integrated circuit chip;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory, the integrated circuit read only memory implemented on the single integrated circuit chip;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses; and

generating processed information in response to the accessed computer operands and in response to the accessed computer instructions;

the act of generating the processed information comprising the acts of:

generating input information,

generating frame loop heading information,

initializing frame loop information in response to the frame loop heading information,

looping through a frame loop in response to the frame loop information,

updating the frame loop information in response to the looping through the frame loop,

generating block loop heading information,

initializing block loop information in response to the block loop heading information and in response to the looping through the frame loop,

looping through a block loop in response to the block loop information,

updating the block loop information in response to the looping through the block loop,

generating sample loop heading information,

initializing sample loop information in response to the sample loop heading information and in response to the looping through the block loop,

looping through a sample loop in response to the sample loop information,

updating the sample loop information in response to the looping through the sample loop,

generating change information in response to the input information and in response to the looping through the sample loop, and

generating output rounded off change information in response to the change information.

--315. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 314, the process further comprising the acts of:

generating machine control information in response to the processed information; and

operating a machine in response to the machine control information.

--316. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 314, the process further comprising the act of communicating information to a remote location in response to the processed information.

--317. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 314, the process further comprising the acts of:

generating display information in response to the processed information; and

displaying information in response to the display information.

--318. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 314, the process further comprising the acts of:

generating graphics information in response to the processed information; and

displaying graphics images in response to the graphics information.

--319. A process of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 314, the process further comprising the act of making a product in response to the processed information.

--320. A process of operating a digital signal processor comprising the acts of:

storing computer operands in an integrated circuit operand memory;

generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

storing a computer program comprising computer instructions in an integrated circuit read only memory and storing an interrupt program comprising interrupt instructions in the integrated circuit read only memory;

generating instruction addresses;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the instruction addresses;

generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

generating input interrupt information;

interrupting the generating of the first processed information in response to the input interrupt information;

writing an interrupt return instruction address into the integrated circuit operand memory in response to the input interrupt information, the integrated circuit operand memory storing the interrupt return instruction address;

generating an input interrupt address;

generating interrupt instruction addresses in response to the input interrupt address;

generating accessed interrupt instructions in response to the interrupt instructions stored in the integrated circuit read only memory and in response to the interrupt instruction addresses;

generating interrupt information in response to the accessed interrupt instructions and generating interrupt return information in response to at least one of the accessed interrupt instructions;

generating an accessed interrupt return instruction address in response to the interrupt return instruction address stored in the integrated circuit operand memory and in response to the interrupt return information;

generating second processed information in response to the accessed computer operands and in response to the accessed computer instructions;

storing an index operand in an integrated circuit index memory;

generating an indexed instruction address in response to the index operand stored in the index memory and in response to at least one of the instruction addresses;

generating accessed indexed computer instructions in response to the computer instructions stored in the integrated circuit read only memory and in response to the indexed instruction address;

generating third processed information in response to the accessed computer operands and in response to the accessed indexed computer instructions;

generating direct transfer information in response to the accessed computer instructions;

generating an accessed directly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory and in response to the direct transfer information;

generating fourth processed information in response to the accessed computer operands and in response to the accessed directly transferred computer instruction;

storing an indirect transfer address in an integrated circuit indirect transfer memory;

generating indirect transfer information in response to the accessed computer instructions;

generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions stored in the integrated circuit read only memory, in response to the indirect transfer address stored in the integrated circuit indirect transfer memory, and in response to the indirect transfer information; and

generating fifth processed information in response to the accessed computer operands and in response to the accessed indirectly transferred computer instruction;

the act of generating the first processed information comprising the acts of:

generating input information,

generating synchronization information,

generating frame loop header information,

initializing frame loop information in response to the frame loop header information and in response to the synchronization information,

looping through a frame loop in response to the frame loop information,

generating updated frame loop information in response to the looping through the frame loop,

generating block loop header information,

initializing block loop information in response to the block loop header information and in response to the updated frame loop information,

looping through a block loop in response to the block loop information,

generating updated block loop information in response to the looping through the block loop,

generating sample loop header information,

initializing sample loop information in response to the sample loop header information and in response to the updated block loop information,

looping through a sample loop in response to the sample loop information,

skipping at least one loop through the sample loop in response to the sample loop information,

generating updated sample loop information in response to the looping through the sample loop,

generating product information in response to the input information and in response to the updated sample loop information, and

generating output rounded off product information in response to the product information.

F24
#1

--321. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 320, the process further comprising the acts of:

generating machine control information in response to the first processed information; and

operating a machine in response to the machine control information.

--322. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 320, the process further comprising the act of communicating information to a remote location in response to the first processed information.

--323. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 320, the process further comprising the acts of:

generating display information in response to the first processed information; and

displaying information in response to the display information.

--324. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 320, the process further comprising the acts of:

generating graphics information in response to the first processed information; and

displaying graphics images in response to the graphics information.

--325. A process of operating a system comprising the process of operating a digital signal processor as set forth in claim 320, the process further comprising the act of making a product in response to the fifth processed information.

--326. A process of operating a digital signal processor system comprising the acts of:

generating keyboard information;

communicating serial keyboard information in response to the keyboard information;

storing computer instructions in an integrated circuit read only memory;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory;

storing computer operands in an integrated circuit alterable memory;

generating accessed computer operands in response to the computer operands stored in the integrated circuit alterable memory;

generating processed information in response to the serial keyboard information, in response to the accessed computer instructions, and in response to the accessed computer operands; and

inputting processed computer operands into the integrated circuit alterable memory in response to the accessed computer instructions and in response to the processed information, the integrated circuit alterable memory storing the processed computer operands.

--327. A process of operating a digital signal processor system as set forth in claim 326, the process further comprising the acts of:

communicating serial display information in response to the processed information; and

displaying machine information in response to the serial display information.

--328. A process of operating a digital signal processor system as set forth in claim 326, the process further comprising the acts of:

communicating first serial machine information, second serial machine information, and third serial machine information in response to the processed information;

inputting first input machine information into a first machine register in response to the first serial machine information, the first machine register storing the first input machine information;

generating first output machine information in response to the first input machine information stored in the first machine register;

performing a first machine operation in response to the first output machine information;

inputting second input machine information into a second machine register in response to the second serial machine information, the second machine register storing the second input machine information;

generating second output machine information in response to the second input machine information stored in the second machine register;

performing a second machine operation in response to the second output machine information;

inputting third input machine information into a third machine register in response to the third serial machine information, the third machine register storing the third input machine information input by the third machine register input circuit;

generating third output machine information in response to the third input machine information stored in the third machine register; and

performing a third machine operation in response to the third output machine information.

--329. A process of operating a digital signal processor system as set forth in claim 326, the process further comprising the acts of:

communicating serial output information in response to the processed information;

generating output machine information in response to the serial output information; and

generating machine information in response to the output machine information.

--330. A process of operating a digital signal processor system as set forth in claim 326, the process further comprising the act of making a product in response to the processed information.

--331. A process of operating a digital signal processor system as set forth in claim 326, the process further comprising the act of generating a photo optical mask in response to processed information.

--332. A process of operating a digital signal processor system as set forth in claim 331, the process further comprising the act of making a product in response to the photo optical mask.

--333. A process of operating a digital signal processor system as set forth in claim 326, the process further comprising the act of generating a pattern in response to processed information.

--334. A process of operating a digital signal processor system as set forth in claim 333, the process further comprising the act of making a product in response to the pattern.

--335. A process of operating a digital signal processor system as set forth in claim 326, the process further comprising the act of generating a plot in response to processed information.

--336. A process of operating a digital signal processor system as set forth in claim 335, the process further comprising the act of making a product in response to the plot.

--337. A process of operating a digital signal processor system comprising the acts of:

generating keyboard information;

communicating serial keyboard information in response to the keyboard information;

storing computer instructions in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

generating accessed computer instructions in response to the computer instructions stored in the integrated circuit read only memory;

storing computer operands in an integrated circuit alterable memory the integrated circuit alterable memory implemented on a single integrated circuit chip;

generating accessed computer operands in response to the computer operands stored in the integrated circuit alterable memory;

generating processed information in response to the serial keyboard information, in response to the accessed computer instructions, and in response to the accessed computer operands; and

inputting processed computer operands into the integrated circuit alterable memory in response to the accessed computer instructions and in response to the processed information, the integrated circuit alterable memory storing the processed computer operands.

--338. A process of operating a digital signal processor system as set forth in claim 337, the process further comprising the acts of:

communicating serial display information in response to the processed information; and

displaying machine information in response to the serial display information.

--339. A process of operating a digital signal processor system as set forth in claim 337, the process further comprising the acts of:

communicating first serial machine information, second serial machine information, and third serial machine information in response to the processed information;

inputting first input machine information into a first machine register in response to the first serial machine information, the first machine register storing the first input machine information;

generating first output machine information in response to the first input machine information stored in the first machine register;

performing a first machine operation in response to the first output machine information;

inputting second input machine information into a second machine register in response to the second serial machine information, the second machine register storing the second input machine information;

generating second output machine information in response to the second input machine information stored in the second machine register;

performing a second machine operation in response to the second output machine information;

inputting third input machine information into a third machine register in response to the third serial machine information, the third machine register storing the third input machine information input by the third machine register input circuit;

generating third output machine information in response to the third input machine information stored in the third machine register; and

performing a third machine operation in response to the third output machine information.

--340. A process of operating a digital signal processor system as set forth in claim 337, the process further comprising the acts of:

communicating serial output information in response to the processed information;

generating output machine information in response to the serial output information; and

generating machine information in response to the output machine information.

--341. A process of operating a digital signal processor system as set forth in claim 337, the process further comprising the act of making a product in response to the processed information.

--342. A process of operating a digital signal processor system as set forth in claim 341, the process further comprising the act of making a product in response to the photo optical mask.

--343. A process of operating a digital signal processor system as set forth in claim 337, the process further comprising the act of generating a pattern in response to processed information.

--344. A process of operating a digital signal processor system as set forth in claim 343, the process further comprising the act of making a product in response to the pattern.

--345. A process of operating a digital signal processor system as set forth in claim 337, the process further comprising the act of generating a plot in response to processed information.

--346. A process of operating a digital signal processor system as set forth in claim 345, the process further comprising the act of making a product in response to the plot.

--347. A digital signal processor system comprising:

means for generating keyboard information;

means for communicating serial keyboard information in response to the keyboard information;

means for storing computer instructions;

means for generating accessed computer instructions in response to the computer instructions;

means for storing computer operands;

means for generating accessed computer operands in response to the computer operands;

means for generating processed information in response to the serial keyboard information, in response to the accessed computer instructions, and in response to the accessed computer operands;

means for storing processed computer operands in response to the accessed computer instructions and in response to the processed information;

means for communicating serial display information in response to the processed information;

means for displaying machine display information in response to the serial display information;

means for communicating serial information in response to the processed information;

means for storing output machine information in response to the serial output information;

means for generating machine output information in response to the output machine information;

means for communicating first serial machine information in response to the processed information, second serial machine information in response to the processed information, and third serial machine information in response to the processed information;

means for storing first input machine information in response to the first serial machine information;

means for generating first output machine information in response to the first input machine information;

means for performing a first machine operation in response to the first output machine information;

means for storing second input machine information in response to the second serial machine information;

means for generating second output machine information in response to the second input machine information;

means for performing a second machine operation in response to the second output machine information;

means for inputting third input machine information in response to the third serial machine information;

means for generating third output machine information in response to the third input machine information; and

means for performing a third machine operation in response to the third output machine information.

--348. A digital signal processor comprising:

means for storing computer operands;

means for generating accessed computer operands in response to the computer operands;

means for storing an interrupt program comprising interrupt instructions;

means for generating instruction addresses;

means for generating accessed computer instructions in response to the computer instructions and in response to the instruction addresses;

means for generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

means for generating display information in response to the first processed information;

means for displaying information in response to the display information;

means for generating input interrupt information;

means for interrupting the generating of the first processed information in response to the input interrupt information;

means for writing an interrupt return instruction address in response to the input interrupt information;

means for generating an input interrupt address;

means for generating interrupt instruction addresses in response to the input interrupt address;

means for generating accessed interrupt instructions in response to the interrupt instructions and in response to the interrupt instruction addresses;

means for generating interrupt return information in response to at least one of the accessed interrupt instructions;

means for generating an accessed interrupt return instruction address in response to the interrupt return instruction address and in response to the interrupt return information;

means for generating second processed information in response to the accessed computer operands and in response to the accessed computer instructions;

means for storing an index operand;

means for generating an indexed instruction address in response to the index operand and in response to at least one of the instruction addresses;

means for generating accessed indexed computer instructions in response to the computer instructions and in response to the indexed instruction address;

means for generating third processed information in response to the accessed computer operands and in response to the accessed indexed computer instructions;

means for generating direct transfer information in response to the accessed computer instructions;

means for generating an accessed directly transferred computer instruction in response to at least one of the computer instructions and in response to the direct transfer information;

means for generating fourth processed information in response to the accessed computer operands and in response to the accessed directly transferred computer instruction;

means for storing an indirect transfer address;

means for generating indirect transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

means for generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions, in response to the indirect transfer address, and in response to the indirect transfer information; and

means for generating fifth processed information in response to the accessed computer operands and in response to the accessed indirectly transferred computer instruction;

means for generating graphics information in response to the fifth processed information; and

means for displaying graphics images in response to the graphics information generated by the graphics circuit.

--349. An integrated circuit digital signal processor implemented on a single integrated circuit chip, the integrated circuit digital signal processor comprising:

means for storing computer operands;

means for generating accessed computer operands in response to the computer operands;

means for storing an interrupt program comprising interrupt instructions;

means for generating instruction addresses;

means for generating accessed computer instructions in response to the computer instructions and in response to the instruction addresses;

means for generating first processed information in response to the accessed computer operands and in response to the accessed computer instructions;

means for communicating information to a remote location in response to the first processed information;

means for generating input interrupt information;

means for interrupting the generating of the first processed information in response to the input interrupt information;

means for writing an interrupt return instruction address in response to the input interrupt information;

means for generating an input interrupt address;

means for generating interrupt instruction addresses in response to the input interrupt address;

means for generating accessed interrupt instructions in response to the interrupt instructions and in response to the interrupt instruction addresses;

means for generating interrupt return information in response to at least one of the accessed interrupt instructions;

means for generating an accessed interrupt return instruction address in response to the interrupt return instruction address and in response to the interrupt return information;

means for generating second processed information in response to the accessed computer operands and in response to the accessed computer instructions;

means for storing an index operand;

means for generating an indexed instruction address in response to the index operand and in response to at least one of the instruction addresses;

means for generating accessed indexed computer instructions in response to the computer instructions and in response to the indexed instruction address;

means for generating third processed information in response to the accessed computer operands and in response to the accessed indexed computer instructions;

means for generating direct transfer information in response to the accessed computer instructions;

means for generating an accessed directly transferred computer instruction in response to at least one of the computer instructions and in response to the direct transfer information;

means for generating fourth processed information in response to the accessed computer operands and in response to the accessed directly transferred computer instruction;

means for storing an indirect transfer address;

means for generating indirect transfer information in response to the accessed computer instructions generated by the integrated circuit read only memory accessing circuit;

means for generating an accessed indirectly transferred computer instruction in response to at least one of the computer instructions, in response to the indirect transfer address, and in response to the indirect transfer information;

means for generating fifth processed information in response to the accessed computer operands and in response to the accessed indirectly transferred computer instruction;

means for generating graphics information in response to the first processed information; and

means for displaying graphics images in response to the graphics information;

the means for generating the first processed information comprising:

means for generating input information;

means for generating synchronization information;

means for generating loop header information;

means for initializing loop information in response to the loop header information and in response to the synchronization information;

means for looping through a loop in response to the loop information;

means for skipping at least one loop through the loop in response to the loop information;

means for updating the loop information in response to the looping through the loop;

means for generating product information in response to the input information and in response to the looping through the loop; and

means for generating output rounded off product information in response to the product information.

--350. An integrated circuit digital signal processor implemented on a single integrated circuit chip, the integrated circuit digital signal processor comprising:

means for storing computer operands;

means for generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

means for storing a computer program comprising computer instructions;

means for generating instruction addresses;

means for generating accessed computer instructions in response to the computer instructions and in response to the instruction addresses;

means for generating processed information in response to the accessed computer operands and in response to the accessed computer instructions;

means for communicating information to a remote location in response to the processed information;

means for generating machine control information in response to the processed information; and

means for operating a machine in response to the machine control information.

--351. A digital signal processor comprising:

means for storing computer operands;

means for generating accessed computer operands in response to the computer operands stored in the integrated circuit operand memory;

means for storing a computer program comprising computer instructions;

means for generating instruction addresses;

means for generating accessed computer instructions in response to the computer instructions and in response to the instruction addresses;

means for generating processed information in response to the accessed computer operands and in response to the accessed computer instructions;

means for generating machine control information in response to the processed information;

means for operating a machine in response to the machine control information;

means for generating display information in response to the processed information; and

means for displaying information in response to the display information;

the means for generating the processed information comprising:

means for generating input information,

means for generating outer loop header information,

means for initializing outer loop information in response to the outer loop header information,

means for looping through an outer loop in response to the outer loop information,

means for generating updated outer loop information in response to the looping through the outer loop,

means for generating middle loop header information,

means for initializing middle loop information in response to the middle loop header information and in response to the updated outer loop information,

means for looping through a middle loop in response to the middle loop information,

means for generating updated middle loop information in response to the looping through the middle loop,

means for generating inner loop header information,

means for initializing inner loop information in response to the inner loop header information and in response to the updated middle loop information,

means for looping through an inner loop in response to the inner loop information,

means for skipping at least one loop through the inner loop in response to the inner loop information,

means for generating updated inner loop information in response to the looping through the inner loop,

means for generating change information in response to the input information and in response to the updated inner loop information, and

means for generating output rounded off change information in response to the change information.